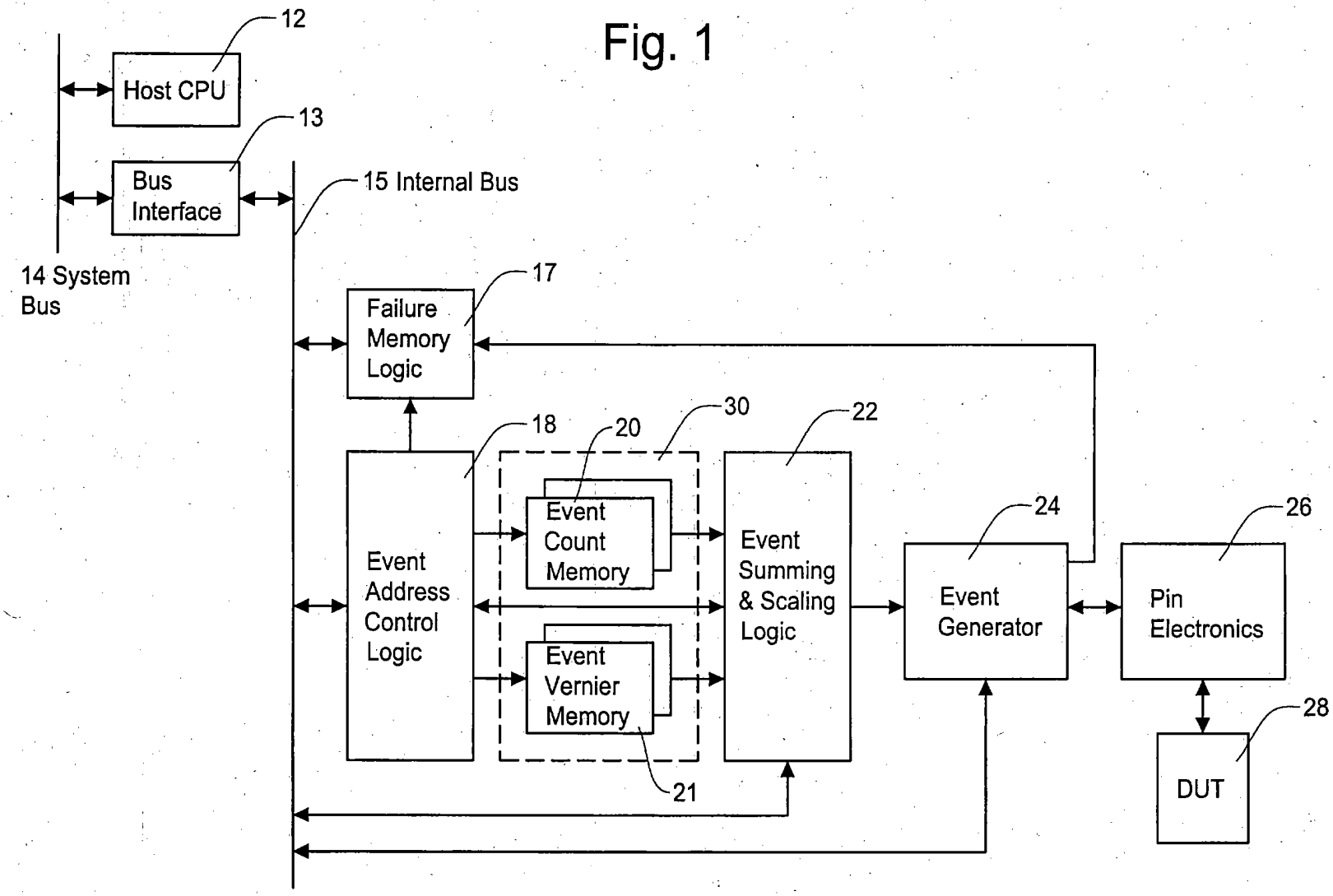
Fig. 1


12
Host CPU
13
Bus Interface
15 Internal Bus
14 System Bus
17
Failure Memory Logic
18
20
30
22
Event Address Control Logic
Event Count Memory
Event Vernier Memory
21
Event Summing & Scaling Logic
24
Event Generator
26
Pin Electronics
28
DUT

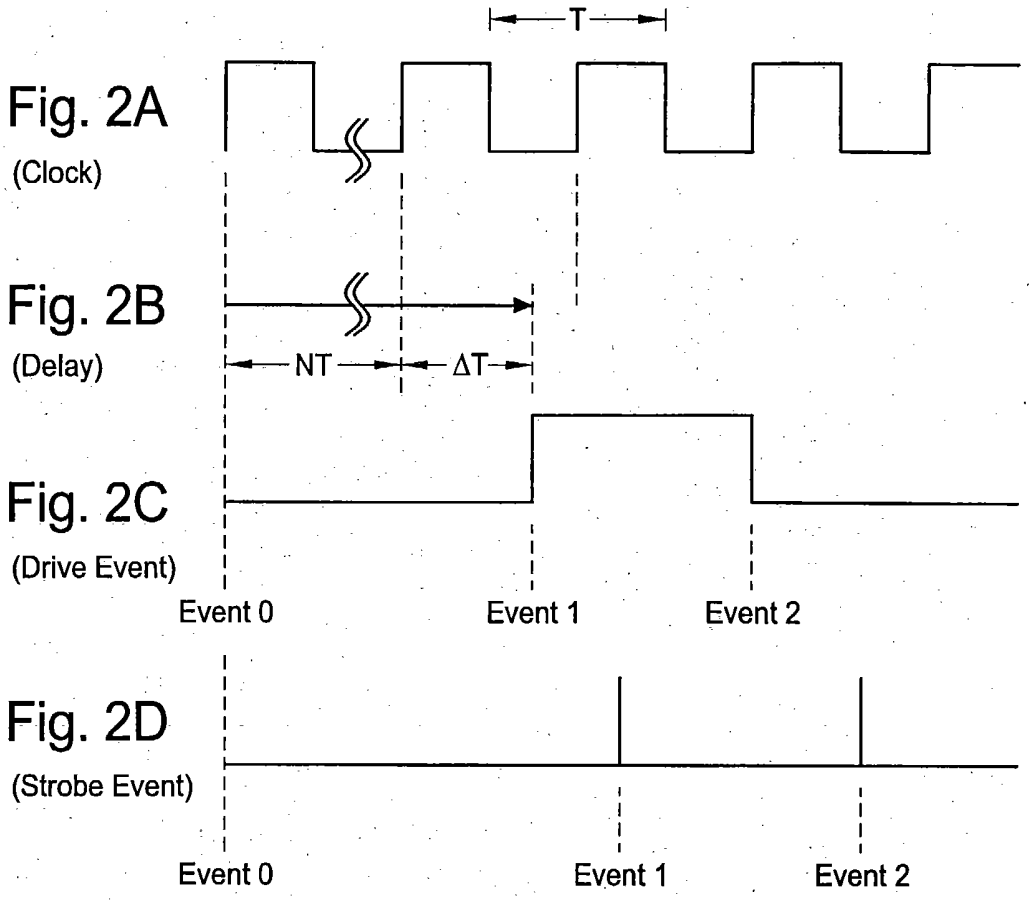

T
Fig. 2A
(Clock)
Fig. 2B
(Delay)
NT
ΔT
Fig. 2C
(Drive Event)
Event 0
Event 1
Event 2
Fig. 2D
(Strobe Event)
Event 0
Event 1
Event 2

Fig. 3

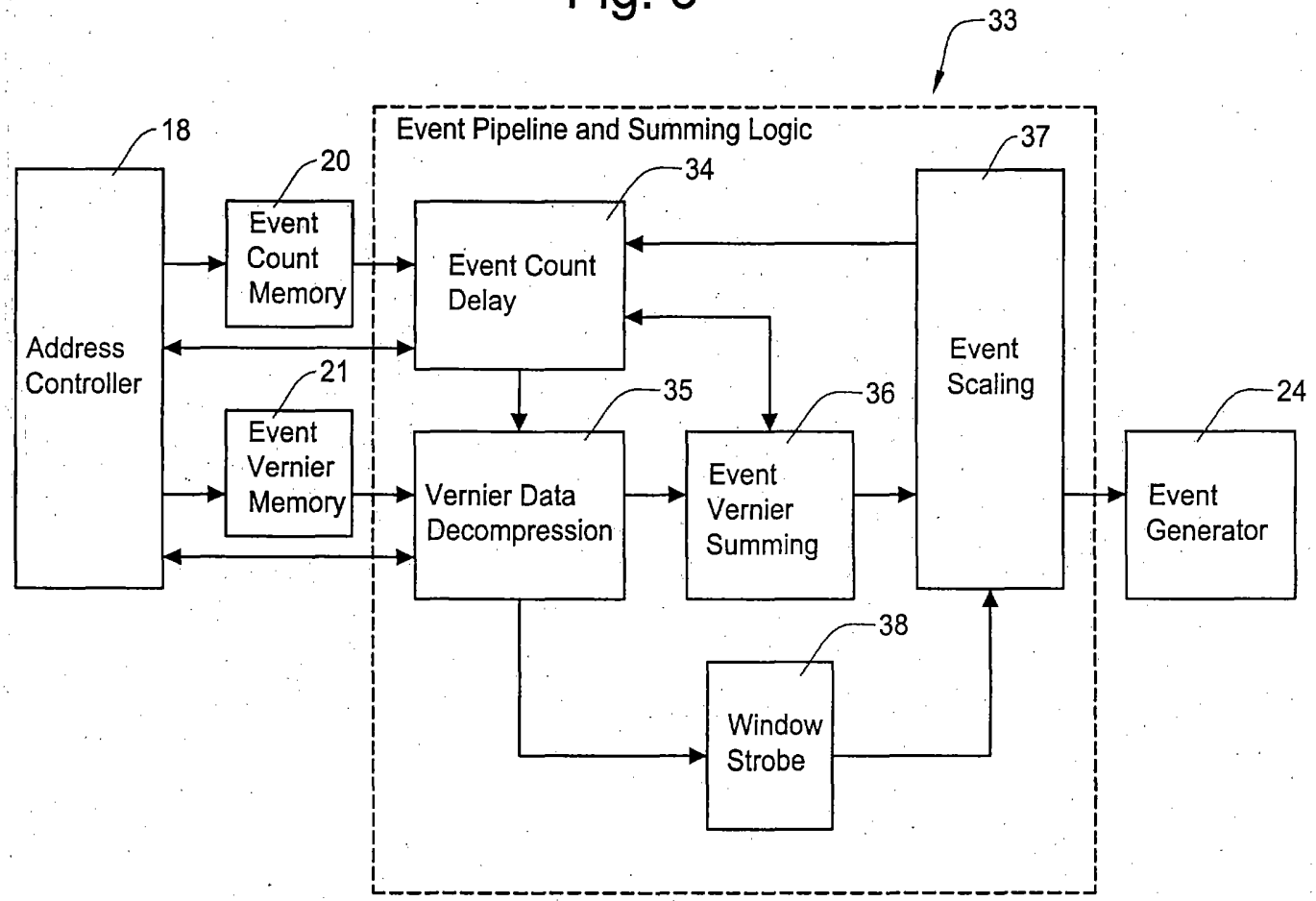

33
Event Pipeline and Summing Logic
18
20
34
37
Event Count Memory
Event Count Delay
Address Controller
Event Scaling
21
35
36
24
Event Vernier Memory
Vernier Data Decompression
Event Vernier Summing
Event Generator
38
Window Strobe

Fig. 4A

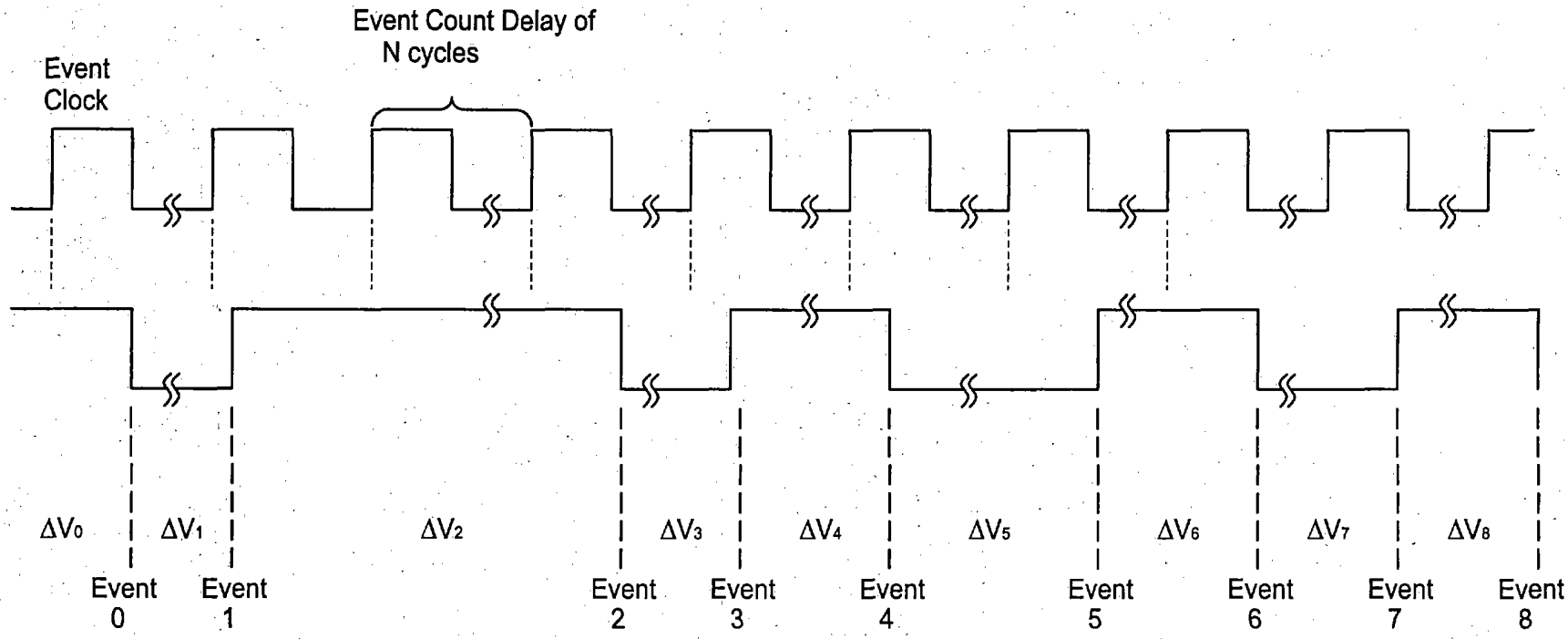

Event Count Delay of
N cycles
Event
Clock
ΔV0
ΔV1
ΔV2
ΔV3
ΔV4
ΔV5
ΔV6
ΔV7
ΔV8
Event
0
Event
1
Event
2
Event
3
Event
4
Event
5
Event
6
Event
7
Event
8

Fig. 4B

Event	Event Count	Event Vernier	Event Type
E0	C0	V0	Drive Low
E1	C1	V1	Drive High
E2	C2	V2	Drive Low
E3	C3	V3	Drive High
E4	C4	V4	Drive Low
E5	C5	V5	Drive High
E6	C6	V6	Drive Low
E7	C7	V7	Drive High
E8	C8	V8	Drive Low

Fig. 5

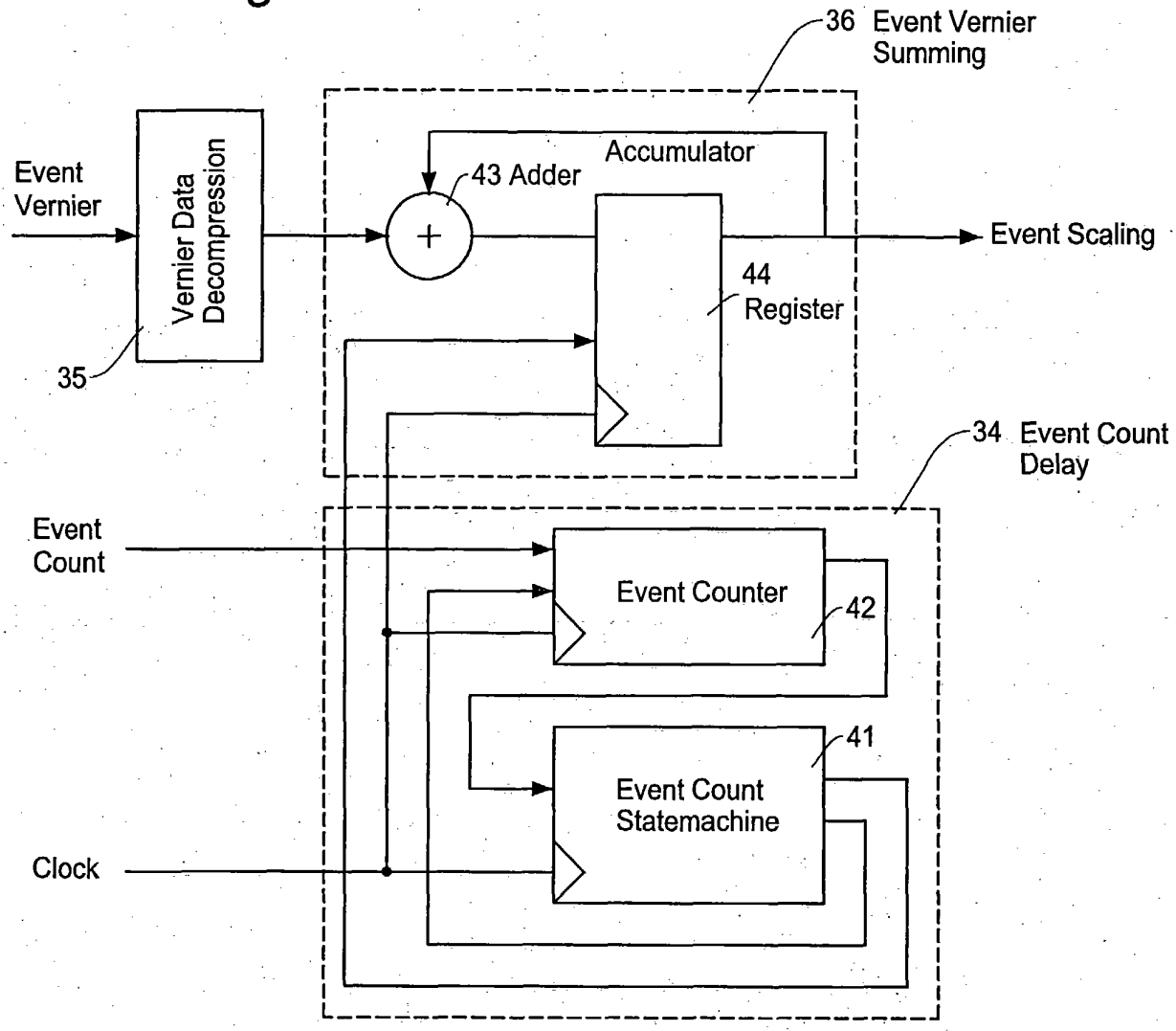

36 Event Vernier Summing
Event Vernier
Vernier Data Decompression
35
43 Adder
Accumulator
Event Scaling
44 Register
34 Event Count Delay
Event Count
Event Counter
42
41
Event Count Statemachine
Clock

Fig. 6A

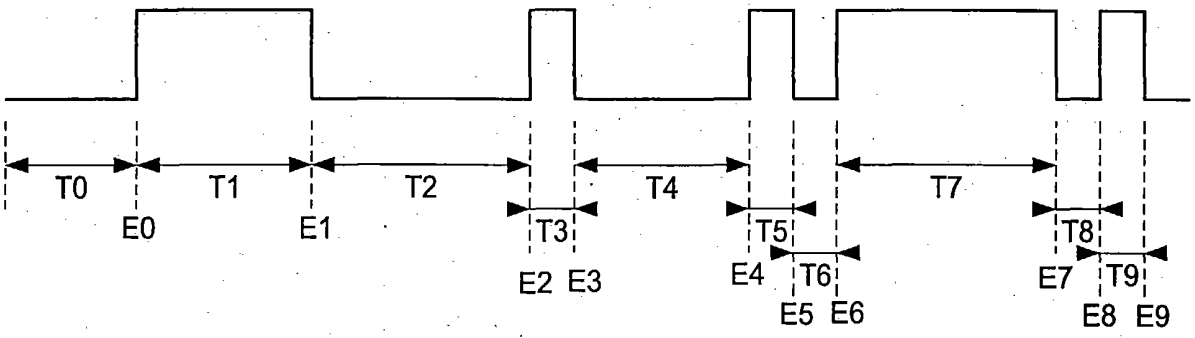


Fig. 6B

Event	Event Count Data	Event Vernier Data
E0	T0 count data	T0 vernier
E1	T1 count data	T1 vernier
E2	T2 count data	T2 vernier
E3	T3 count data	T3 vernier
E4	T4 count data	T4 vernier
E5	T5 count data	T5 vernier
E6	T6 count data	T6 vernier
E7	T7 count data	T7 vernier
E8	T8 count data	T8 vernier
E9	T9 count data	T9 vernier

Fig. 6C

Event	Event Count Memory	Event Vernier Memory
E0	T0 count data (Word 0)	0, 0, 0, T0 vernier
E1	T1 count data (Word 0)	0, T2 vernier, 0, T1 vernier
	T1 count data (Word 1)	T4 vernier, 0, 0, T3 vernier
E2, E3	T2 count data (Word 0)	0, 0, T6 vernier, T5 vernier
	T2 count data (Word 1)	0, T9 vernier, T8 vernier, T7 vernier
	T2 count data (Word 2)	(next vernier data)
E4, E5, E6	T4 count data (Word 0)	(next vernier data)
	T4 count data (Word 1)	(next vernier data)
	T4 count data (Word 2)	(next vernier data)
	T4 count data (Word 3)	(next vernier data)
E7, E8, E9	T7 count data (Word 0)	(next vernier data)

Fig. 7

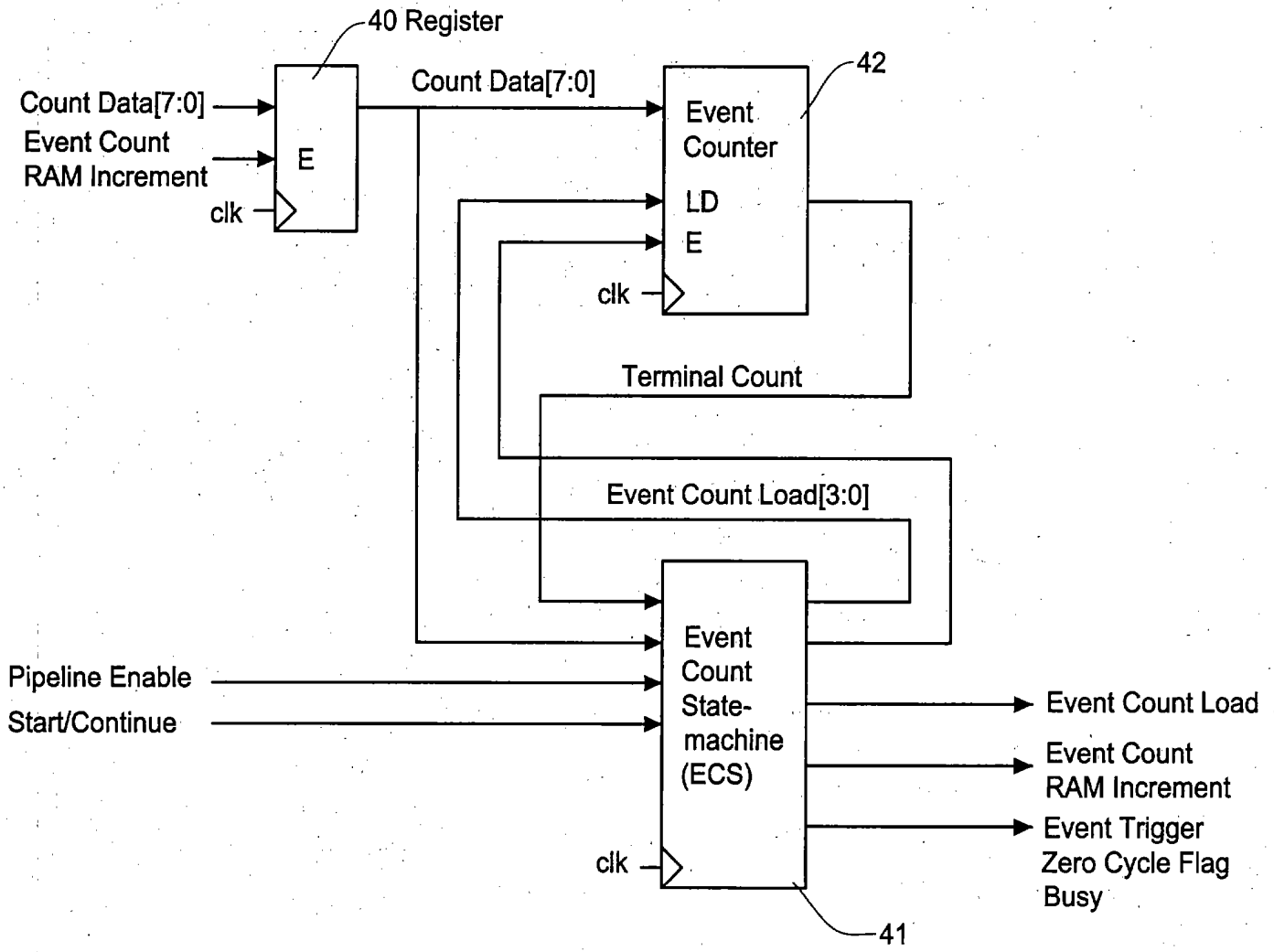

40 Register
Count Data[7:0]
Event Count
RAM Increment
clk
E
Count Data[7:0]
42
Event
Counter
LD
E
clk
Terminal Count
Event Count Load[3:0]
Pipeline Enable
Start/Continue
Event
Count
State-
machine
(ECS)
clk
Event Count Load
Event Count
RAM Increment
Event Trigger
Zero Cycle Flag
Busy
41

Fig. 8

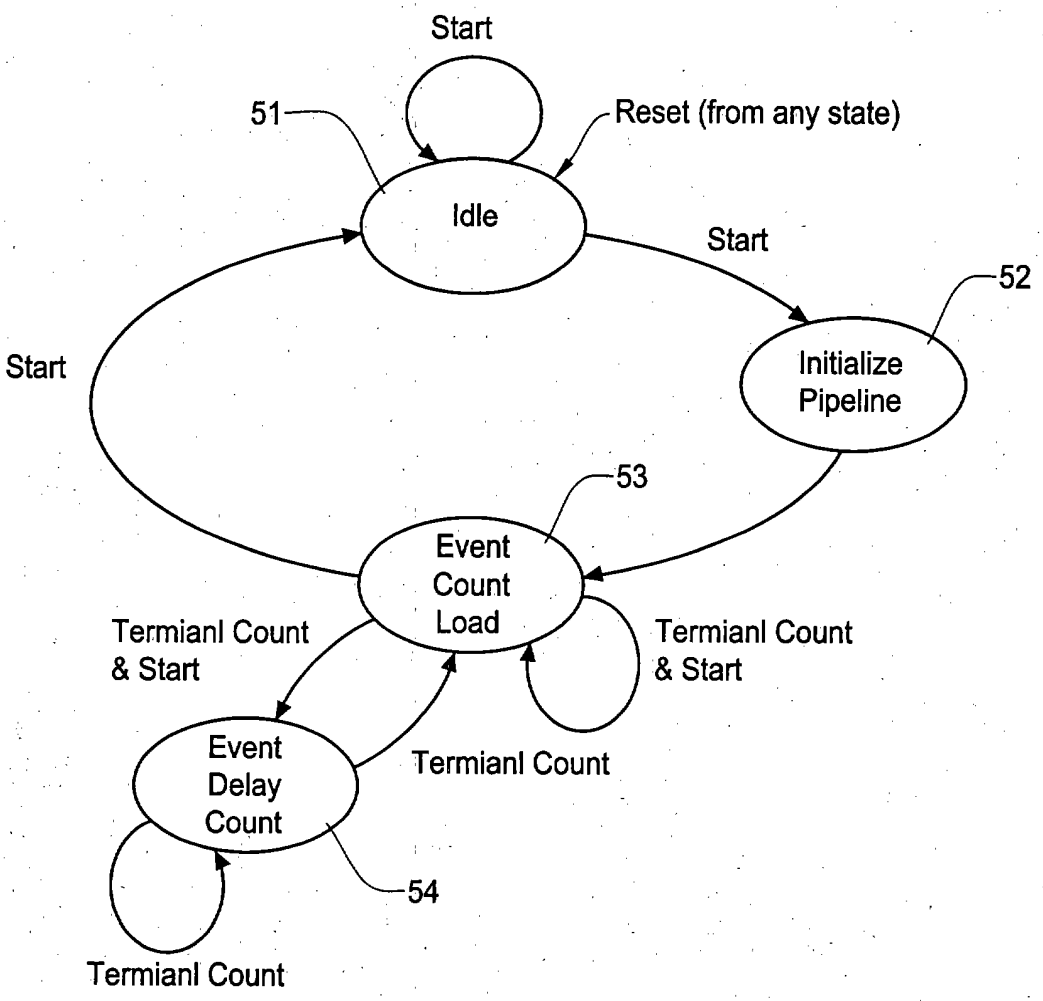

Start
51
Reset (from any state)
Idle
Start
52
Initialize
Pipeline
Start
53
Event
Count
Load
Termianl Count
& Start
Termianl Count
& Start
Event
Delay
Count
Termianl Count
54
Termianl Count

Fig. 9

Address	Bit[7]	Bit[6:5]	Bit[4:0]
Single Word			
N	0	EVCNT[1:0]	COUNT[4:0]
Double Word			
N	0	EVCNT[1:0]	COUNT[4:0]
N+1	1	COUNT[11:10]	COUNT[9:5]
Triple Word			
N	0	EVCNT[1:0]	COUNT[4:0]
N+1	0	COUNT[11:10]	COUNT[9:5]
N+2	1	COUNT[18:17]	COUNT[16:12]
Quad Word			
N	0	EVCNT[1:0]	COUNT[4:0]
N+1	0	COUNT[11:10]	COUNT[9:5]
N+2	0	COUNT[18:17]	COUNT[16:12]
N+3	1	COUNT[25:24]	COUNT[23:19]

Fig. 10

Address	Vernier Pipeline 0	Vernier Pipeline 1	Vernier Pipeline 2	Vernier Pipeline 3
0x0	Event 0, Vernier 0	Event 0, Vernier 1	Event 0, Vernier 2	Event 1, Vernier 0
0x1	Event 1, Vernier 1	Event 1, Vernier 2	Event 1, Vernier 3	Event 2, Vernier 0
0x2	Event 3, Vernier 0	Event 4, Vernier 0	Event 4, Vernier 1	Event 5, Vernier 0
0x3	Event 5, Vernier 1	Event 5, Vernier 2	Event 6, Vernier 0	Event 6, Vernier 1
0x4	Event 7, Vernier 0	Event 7, Vernier 1	Event 8, Vernier 0	Event 9, Vernier 0

Fig. 11

Event Number	EVCNT [1:0]	ECR Address	EVR Address	Vernier Pipeline 0	Vernier Pipeline 1	Vernier Pipeline 2	Vernier Pipeline 3
0	0x2	0x0	0x0	Vernier 0	Vernier 1	Vernier 2	
1	0x3	0x1	0x0-0x1	Vernier 1	Vernier 2	Vernier 3	Vernier 0
2	0x0	0x2	0x1				Vernier 0
3	0x0	0x3	0x2	Vernier 0			
4	0x1	0x4	0x2		Vernier 0	Vernier 1	
5	0x2	0x5	0x2-0x3	Vernier 1	Vernier 2		Vernier 0
6	0x1	0x6	0x3			Vernier 0	Vernier 1
7	0x1	0x7	0x4	Vernier 0	Vernier 1		
8	0x0	0x8	0x4			Vernier 0	
9	0x0	0x9	0x4				Vernier 0

Fig. 12A

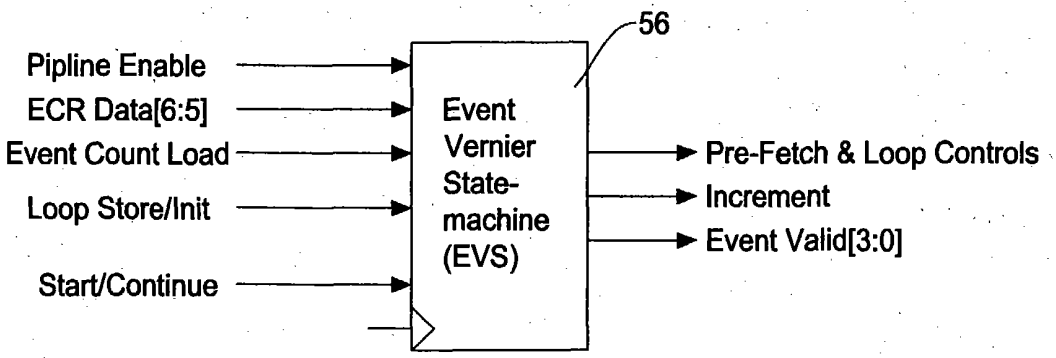


Fig. 12B

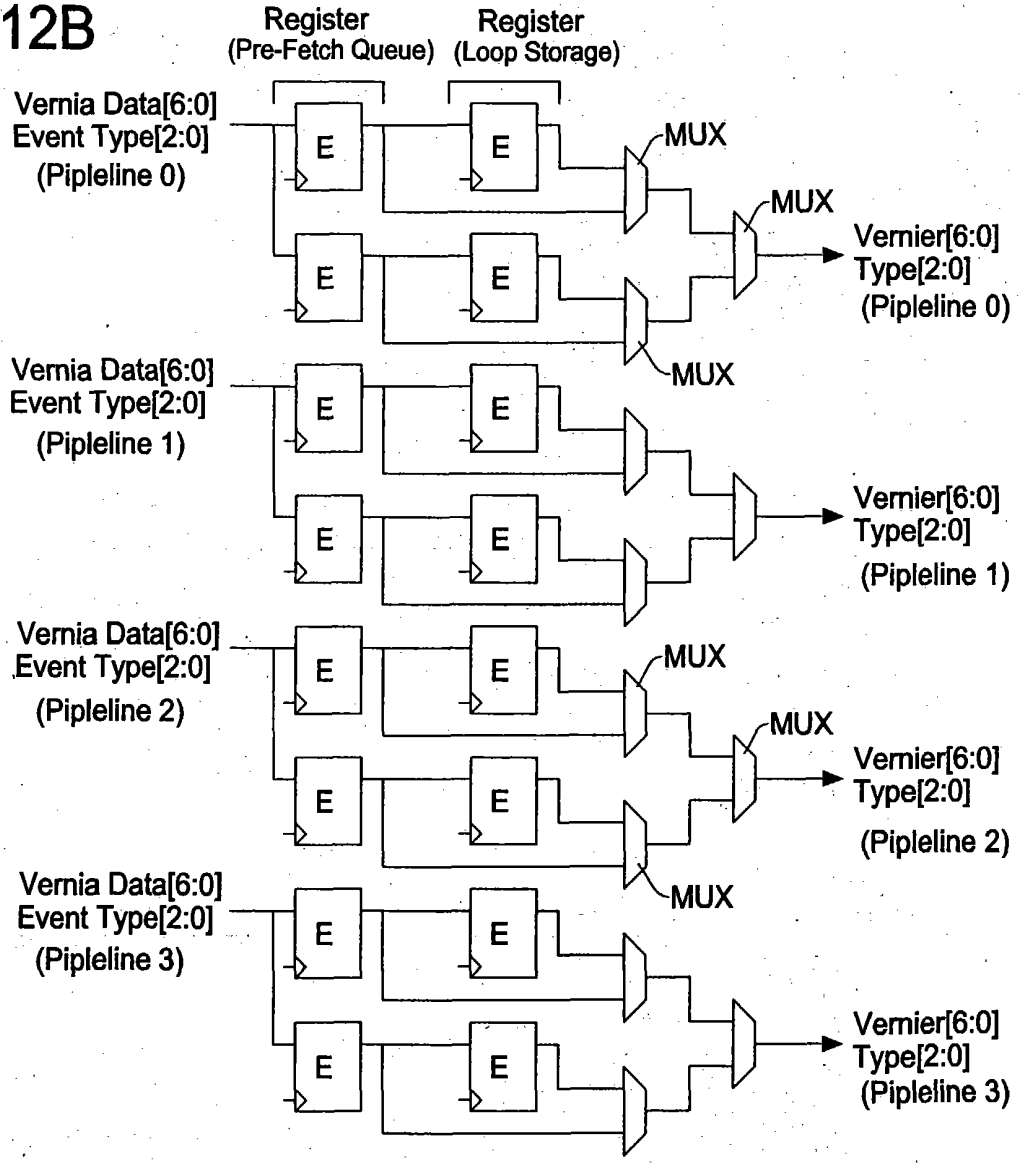


Fig. 13

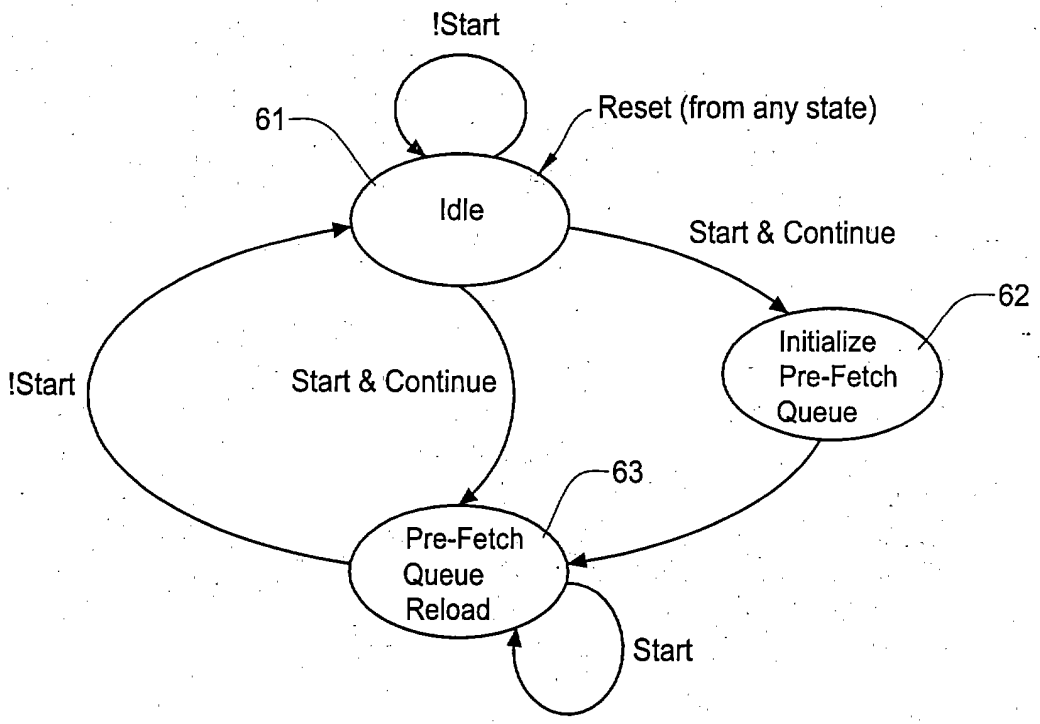

!Start
61
Reset (from any state)
Idle
Start & Continue
62
Initialize
Pre-Fetch
Queue
!Start
Start & Continue
63
Pre-Fetch
Queue
Reload
Start

Fig. 14

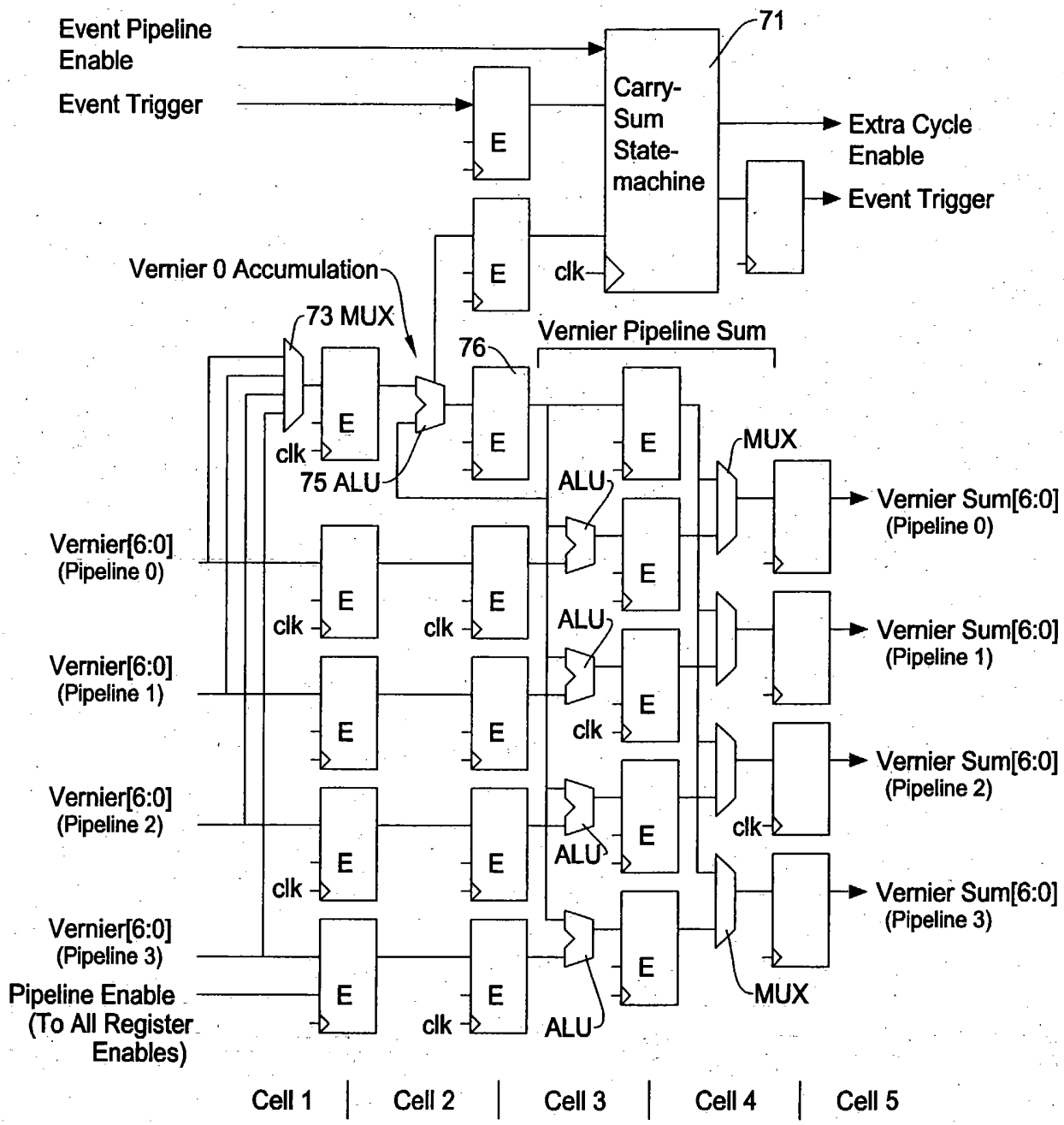

Event Pipeline Enable
Event Trigger
E
71
Carry-Sum State-machine
Extra Cycle Enable
Event Trigger
Vernier 0 Accumulation
clk
73 MUX
Vernier Pipeline Sum
76
E
clk
75 ALU
MUX
ALU
Vernier[6:0] (Pipeline 0)
Vernier Sum[6:0] (Pipeline 0)
Vernier[6:0] (Pipeline 1)
Vernier Sum[6:0] (Pipeline 1)
Vernier[6:0] (Pipeline 2)
Vernier Sum[6:0] (Pipeline 2)
Vernier[6:0] (Pipeline 3)
Vernier Sum[6:0] (Pipeline 3)
Pipeline Enable (To All Register Enables)
Cell 1
Cell 2
Cell 3
Cell 4
Cell 5

Fig. 15

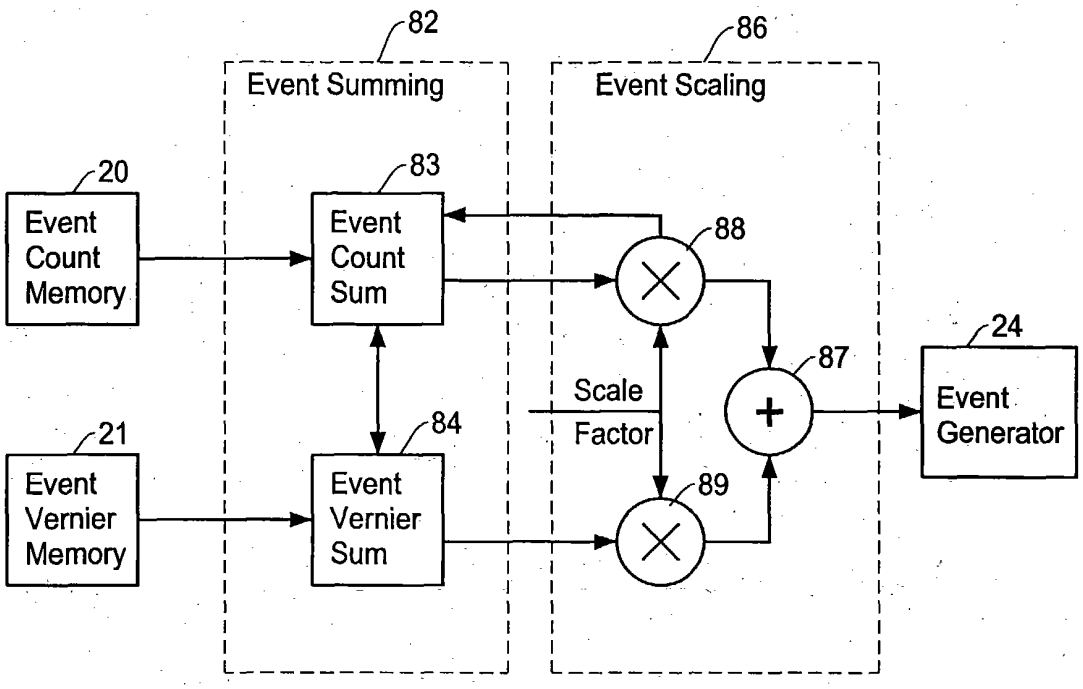

82
Event Summing
86
Event Scaling
20
Event
Count
Memory
83
Event
Count
Sum
88
24
87
Scale
Factor
Event
Generator
21
Event
Vernier
Memory
84
Event
Vernier
Sum
89

Fig. 16

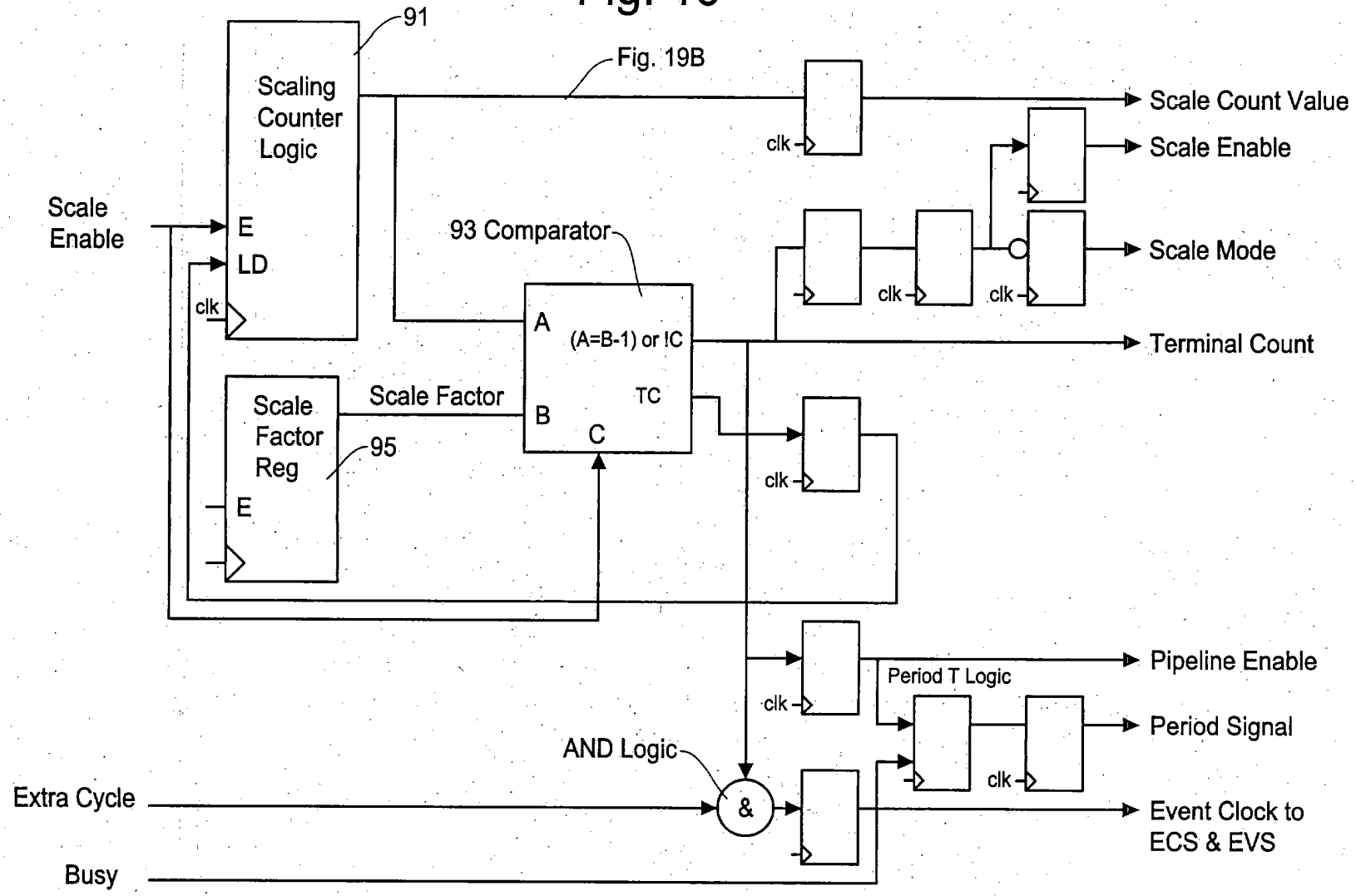

91
Scaling Counter Logic
Fig. 19B
Scale Enable
E
LD
clk
93 Comparator
A
(A=B-1) or !C
TC
B
C
Scale Factor
Scale Factor Reg
95
E
clk
Scale Count Value
Scale Enable
Scale Mode
Terminal Count
Pipeline Enable
Period T Logic
Period Signal
AND Logic
&
Extra Cycle
Busy
Event Clock to ECS & EVS

Fig. 17

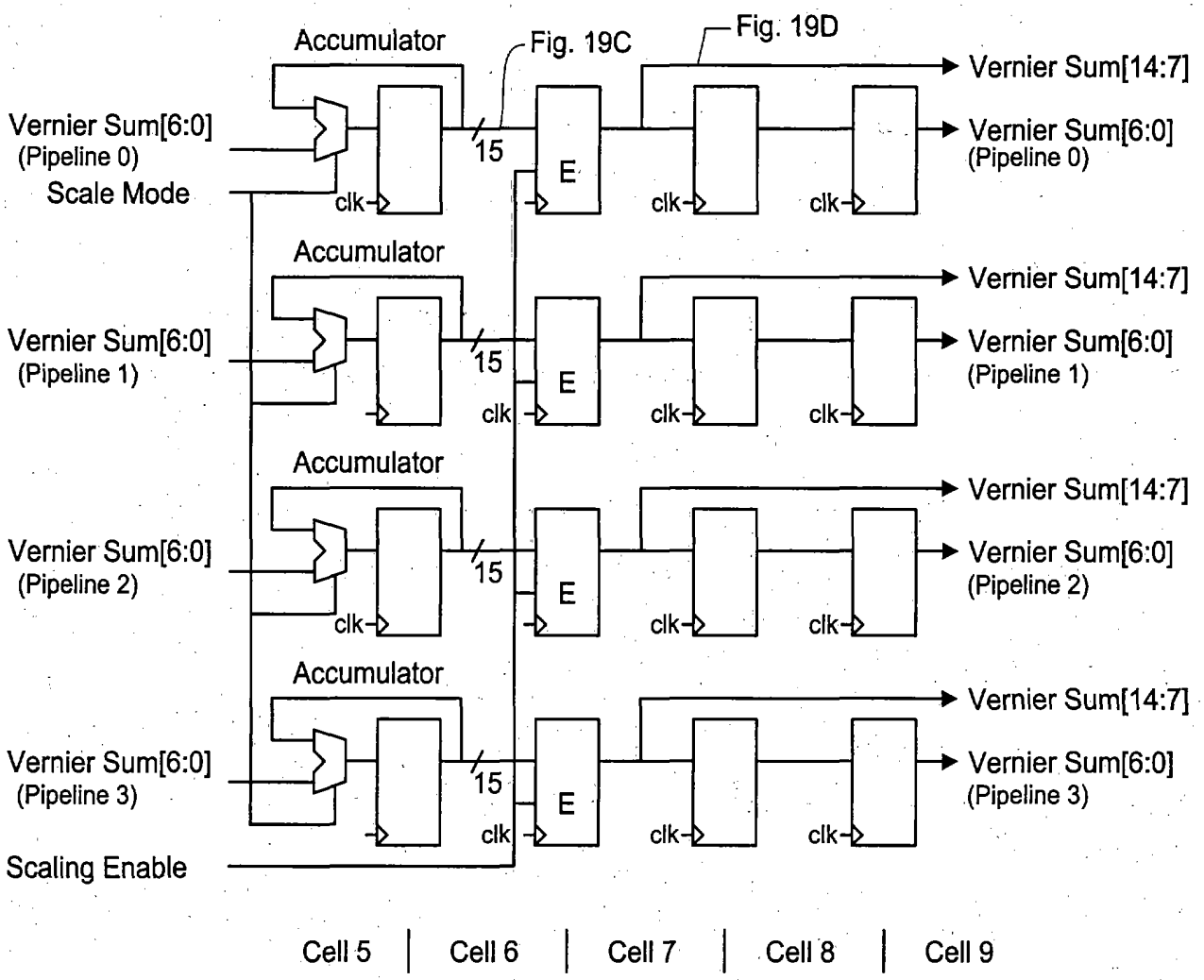
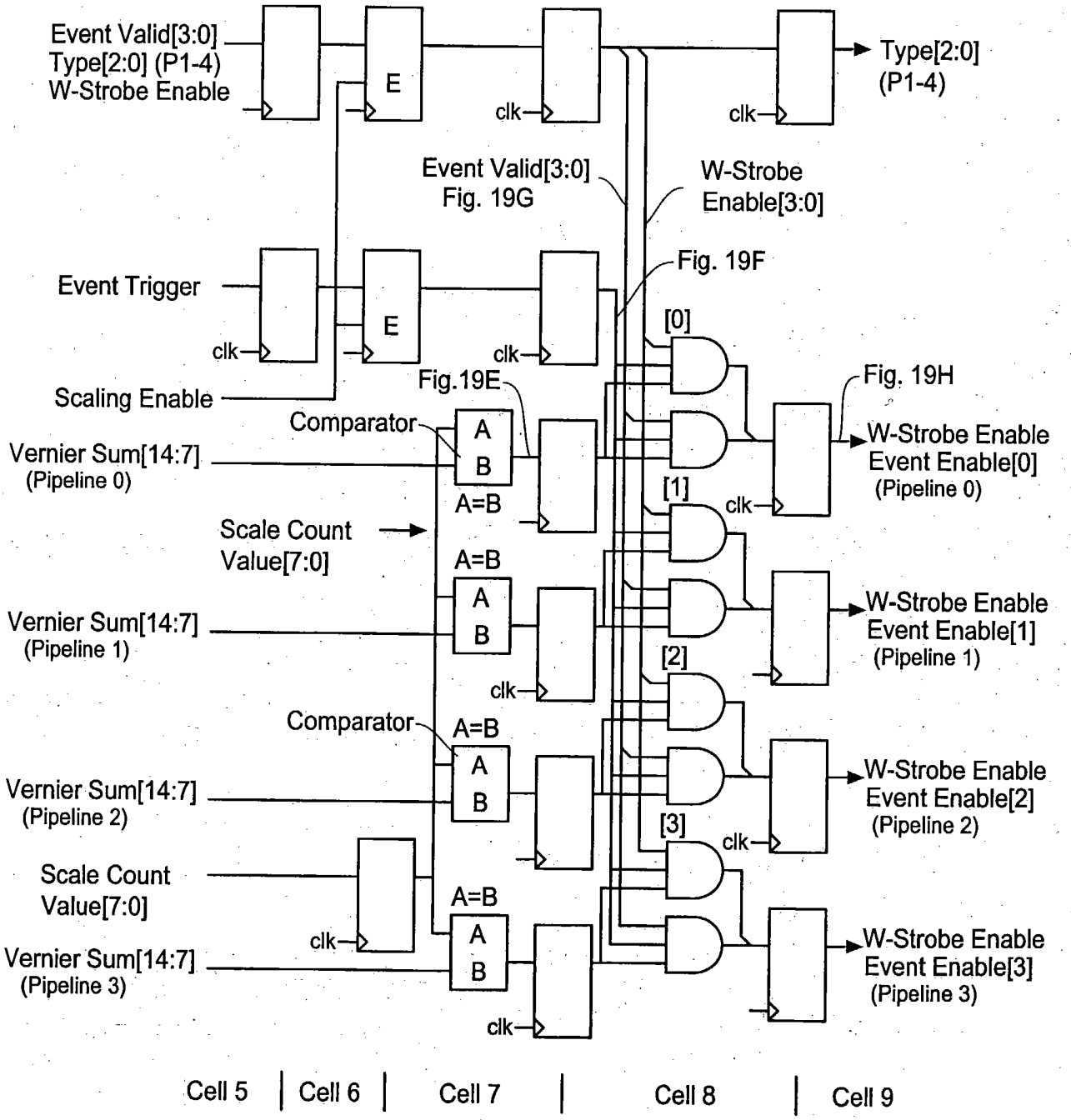
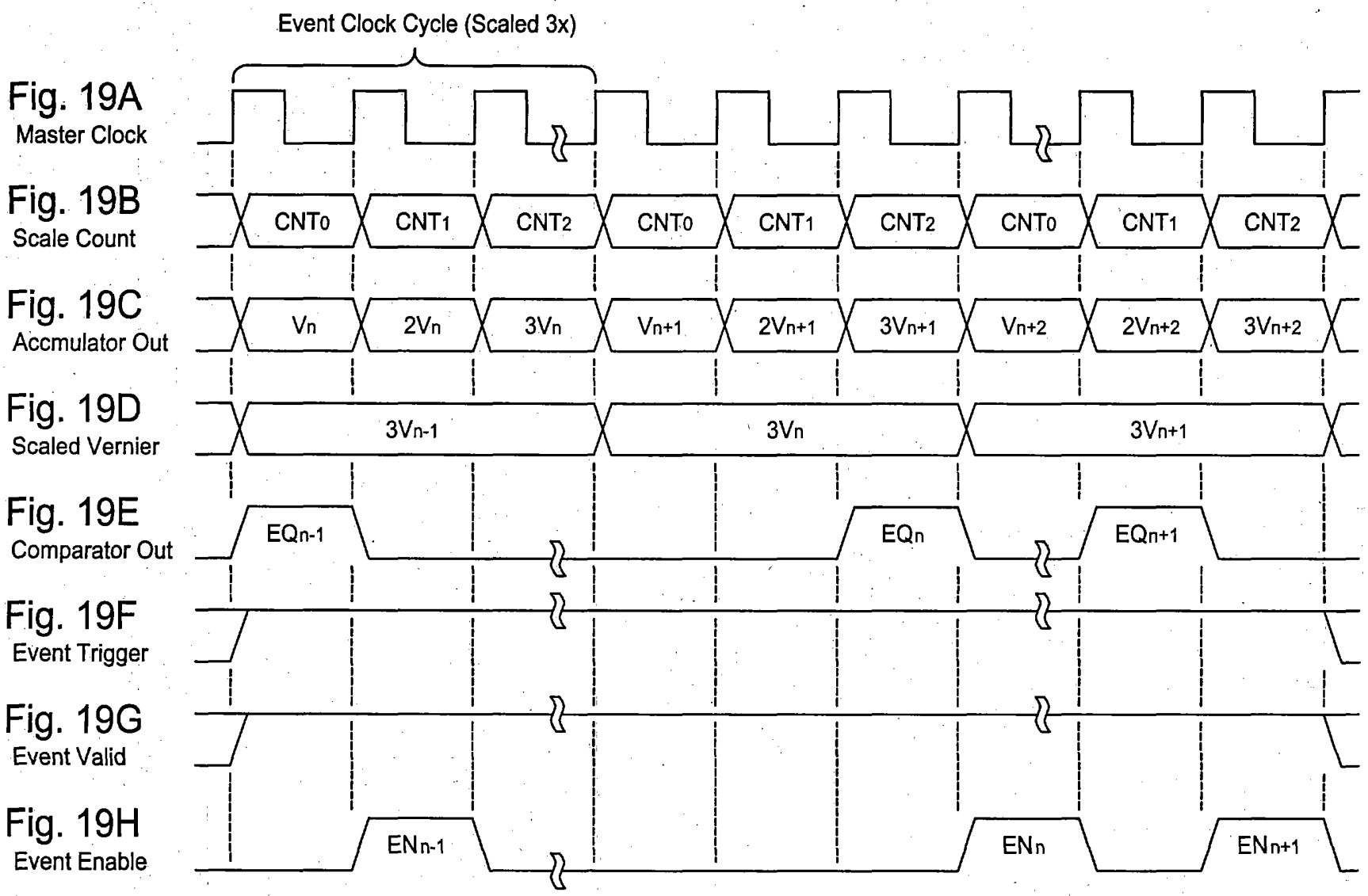

Accumulator
Fig. 19C
Fig. 19D
Vernier Sum[14:7]
Vernier Sum[6:0]
(Pipeline 0)
Scale Mode
15
E
clk
Vernier Sum[6:0]
(Pipeline 0)
Accumulator
Vernier Sum[14:7]
Vernier Sum[6:0]
(Pipeline 1)
Vernier Sum[6:0]
(Pipeline 1)
Accumulator
Vernier Sum[14:7]
Vernier Sum[6:0]
(Pipeline 2)
Vernier Sum[6:0]
(Pipeline 2)
Accumulator
Vernier Sum[14:7]
Vernier Sum[6:0]
(Pipeline 3)
Vernier Sum[6:0]
(Pipeline 3)
Scaling Enable
Cell 5
Cell 6
Cell 7
Cell 8
Cell 9

Fig. 18


Event Valid[3:0]
Type[2:0] (P1-4)
W-Strobe Enable
E
clk
clk
Type[2:0]
(P1-4)
Event Valid[3:0]
Fig. 19G
W-Strobe
Enable[3:0]
Fig. 19F
Event Trigger
clk
E
clk
[0]
Fig. 19E
Fig. 19H
Scaling Enable
Comparator
A
B
A=B
W-Strobe Enable
Event Enable[0]
(Pipeline 0)
Vernier Sum[14:7]
(Pipeline 0)
[1]
clk
Scale Count
Value[7:0]
A=B
A
B
W-Strobe Enable
Event Enable[1]
(Pipeline 1)
Vernier Sum[14:7]
(Pipeline 1)
[2]
clk
Comparator
A=B
A
B
W-Strobe Enable
Event Enable[2]
(Pipeline 2)
Vernier Sum[14:7]
(Pipeline 2)
[3]
clk
Scale Count
Value[7:0]
A=B
A
B
clk
W-Strobe Enable
Event Enable[3]
(Pipeline 3)
Vernier Sum[14:7]
(Pipeline 3)
clk
Cell 5
Cell 6
Cell 7
Cell 8
Cell 9


Event Clock Cycle (Scaled 3x)
Fig. 19A
Master Clock
Fig. 19B
Scale Count
CNT0
CNT1
CNT2
CNT0
CNT1
CNT2
CNT0
CNT1
CNT2
Fig. 19C
Accmulator Out
Vn
2Vn
3Vn
Vn+1
2Vn+1
3Vn+1
Vn+2
2Vn+2
3Vn+2
Fig. 19D
Scaled Vernier
3Vn-1
3Vn
3Vn+1
Fig. 19E
Comparator Out
EQn-1
EQn
EQn+1
Fig. 19F
Event Trigger
Fig. 19G
Event Valid
Fig. 19H
Event Enable
ENn-1
ENn
ENn+1

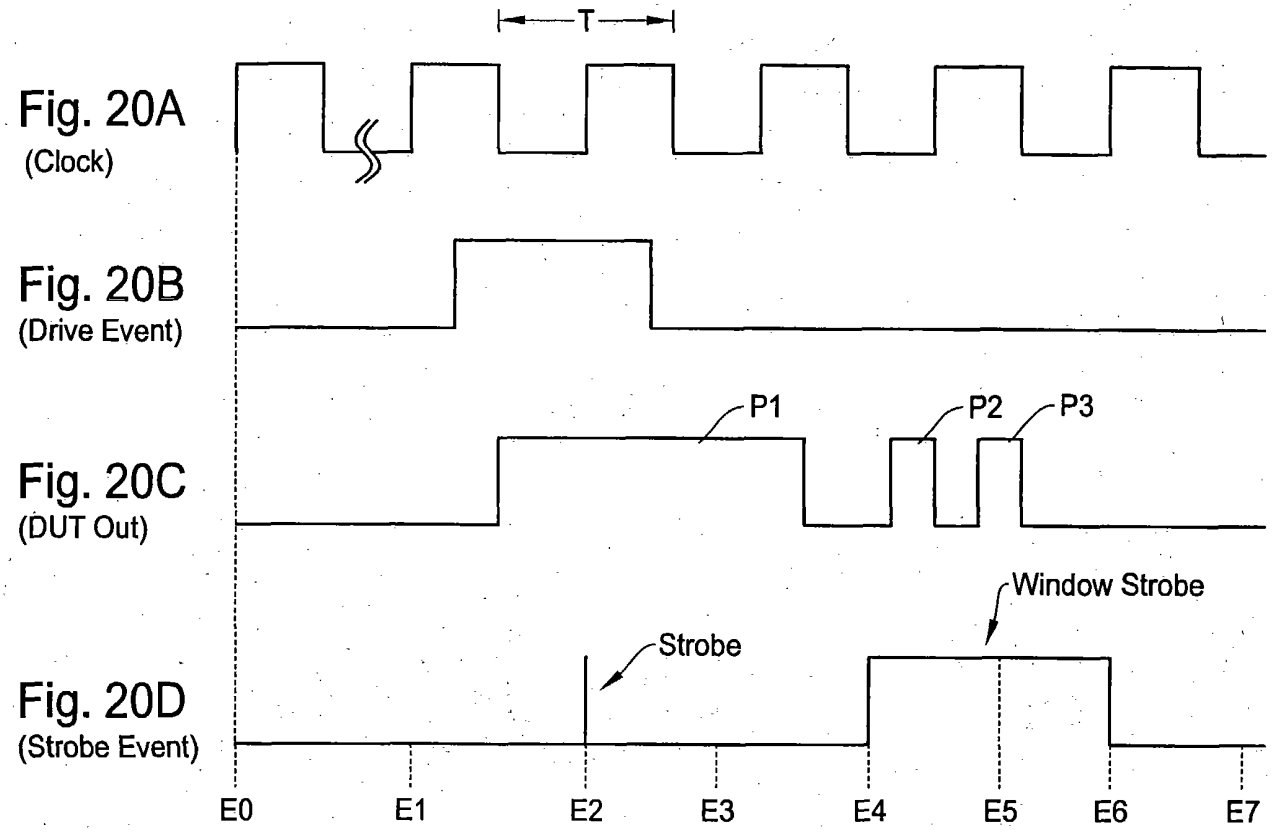


Fig. 21

Event	Event Count	Event Vernier	Event Type
E0	C0	V0	Drive Low
E1	C1	V1	Drive Low
E2	C2	V2	Strobe
E3	C3	V3	Drive Low
E4	C4	V4	Strobe
E5	C5	V5	Strobe
E6	C6	V6	Drive Low
E7	C7	V7	Drive Low

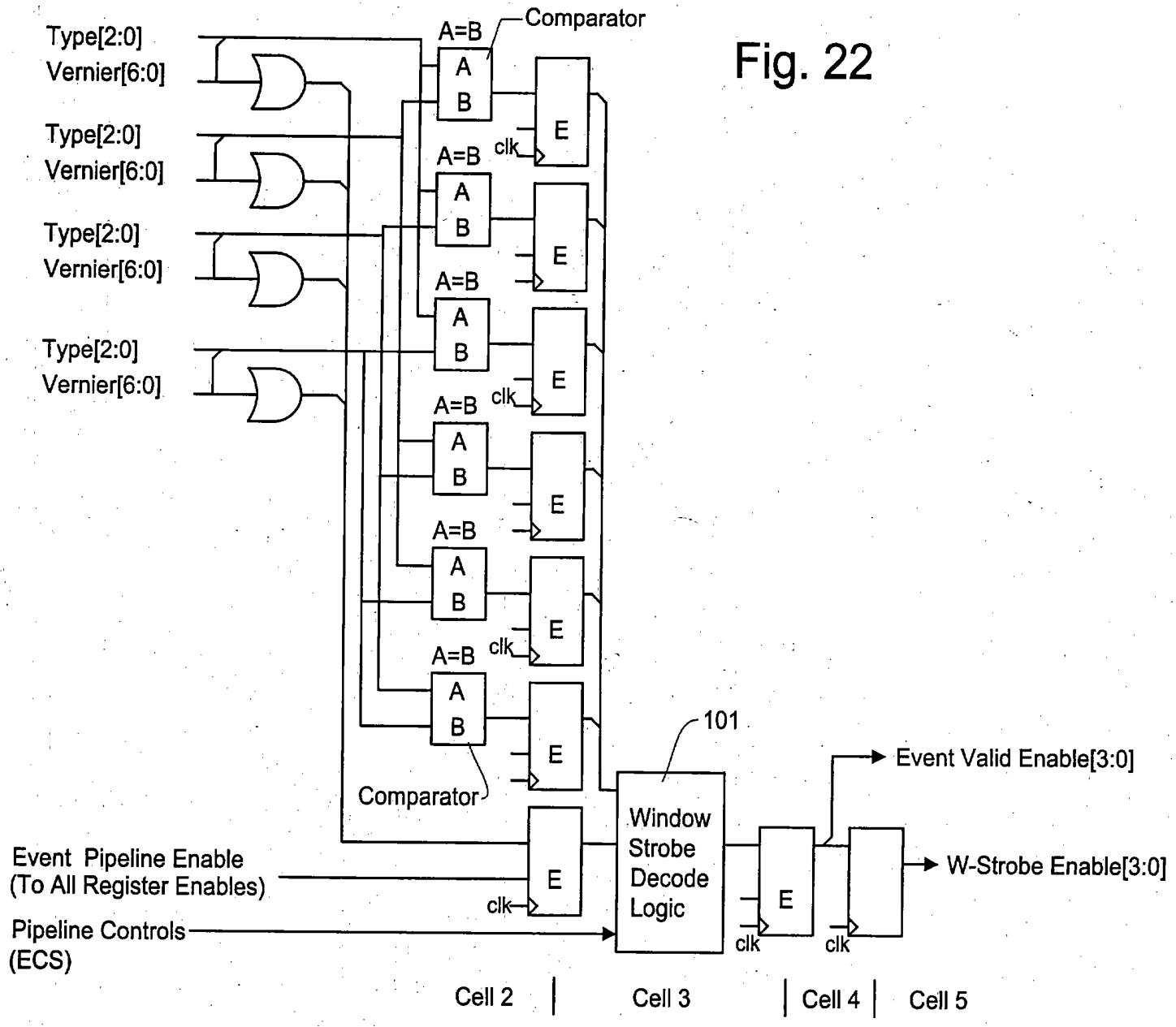

Type[2:0]
Vernier[6:0]
Type[2:0]
Vernier[6:0]
Type[2:0]
Vernier[6:0]
Type[2:0]
Vernier[6:0]
A=B
Comparator
A
B
E
clk
Comparator
101
Window
Strobe
Decode
Logic
Event Valid Enable[3:0]
W-Strobe Enable[3:0]
Event Pipeline Enable
(To All Register Enables)
Pipeline Controls
(ECS)
Cell 2
Cell 3
Cell 4
Cell 5

Fig. 22

Fig. 23A

Window Strobe Type Comparisons				
	Type 0	Type 1	Type 2	Type 3
Type 0		X	X	X
Type 1	X		X	X
Type 2	X	X		
Type 3	X	X	X	

Fig. 23B

Window Strobe Vernier Comparisons				
	Vernier 0	Vernier 1	Vernier 2	Vernier 3
Vernier 0		X	X	X
Vernier 1	X		X	X
Vernier 2	X	X		
Vernier 3	X	X	X	

Fig. 24A

Window Strobe Determinations for Vernier 0					
		Type 0	Type 1	Type 2	Type 3
Vernier = 0	Type 0		W	W	W
	Type 1				
	Type 2				
	Type 3				
Vernier ≠ 0	Type 0				
	Type 1				
	Type 2				
	Type 3				

Fig. 24B

Window Strobe Determinations for Verniers 1, 2, and 3					
		Type 0	Type 1	Type 2	Type 3
Matching Verniers	Type 0				
	Type 1			W	W
	Type 2		W		W
	Type 3		W	W	
No Matching Verniers	Type 0				
	Type 1				
	Type 2				
	Type 3				

Fig. 25

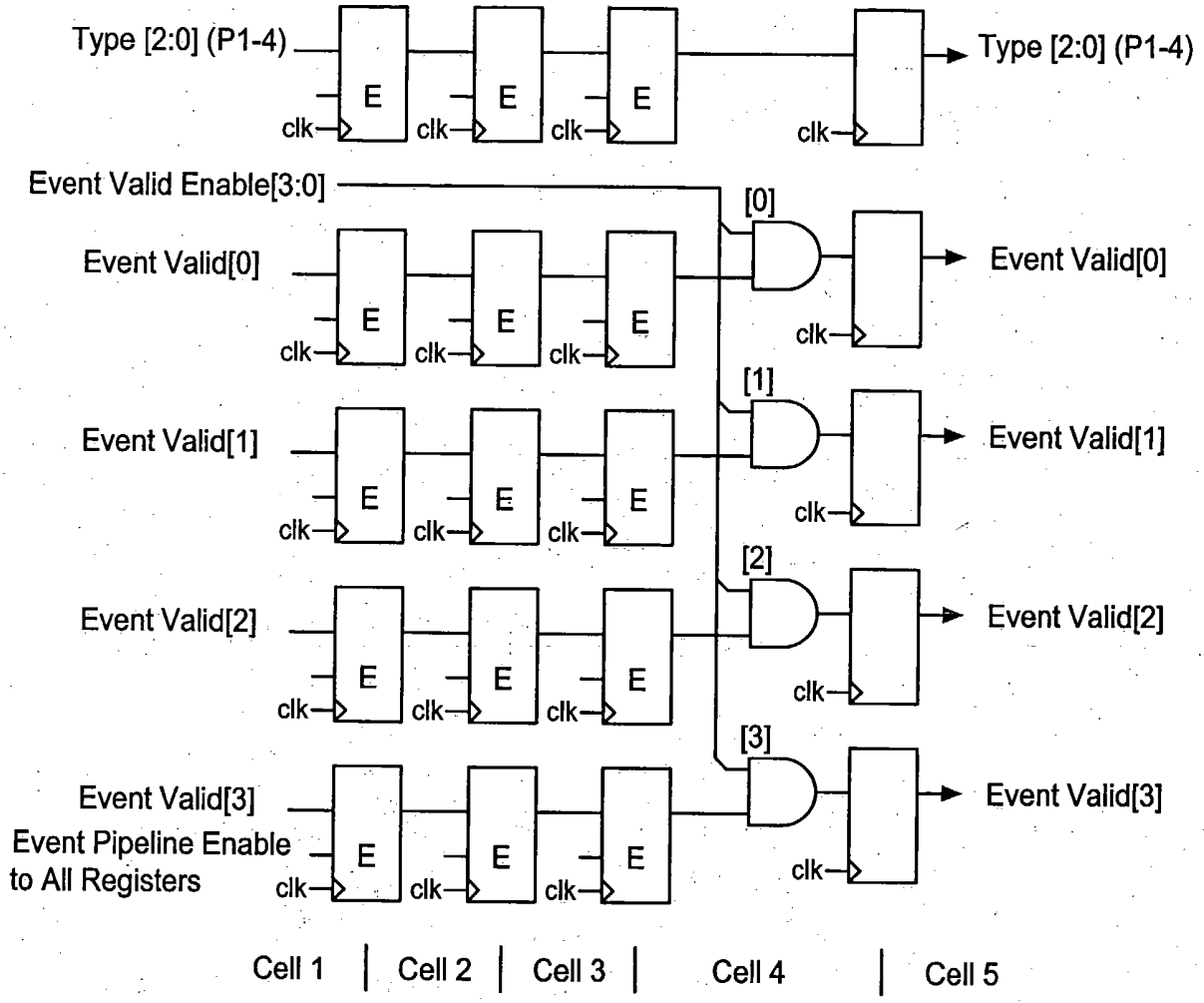

Type [2:0] (P1-4)
E
clk
Type [2:0] (P1-4)
Event Valid Enable[3:0]
[0]
Event Valid[0]
Event Valid[0]
[1]
Event Valid[1]
Event Valid[1]
[2]
Event Valid[2]
Event Valid[2]
[3]
Event Valid[3]
Event Valid[3]
Event Pipeline Enable
to All Registers
Cell 1
Cell 2
Cell 3
Cell 4
Cell 5

Fig. 26

Window Strobe Event Type Removals					
		Type 0	Type 1	Type 2	Type 3
Vernier = 0	Type 0		*Type 1*	*Type 2*	*Type 3*
	Type 1				
	Type 2				
	Type 3				
Vernier ≠ 0	Type 0				
	Type 1				
	Type 2				
	Type 3				
Matching Verniers	Type 0				
	Type 1			*Type 2*	*Type 3*
	Type 2		*Type 1*		*Type 3*
	Type 3		*Type 1*	*Type 3*	
No Matching Verniers	Type 0				
	Type 1				
	Type 2				
	Type 3				

Fig. 27A

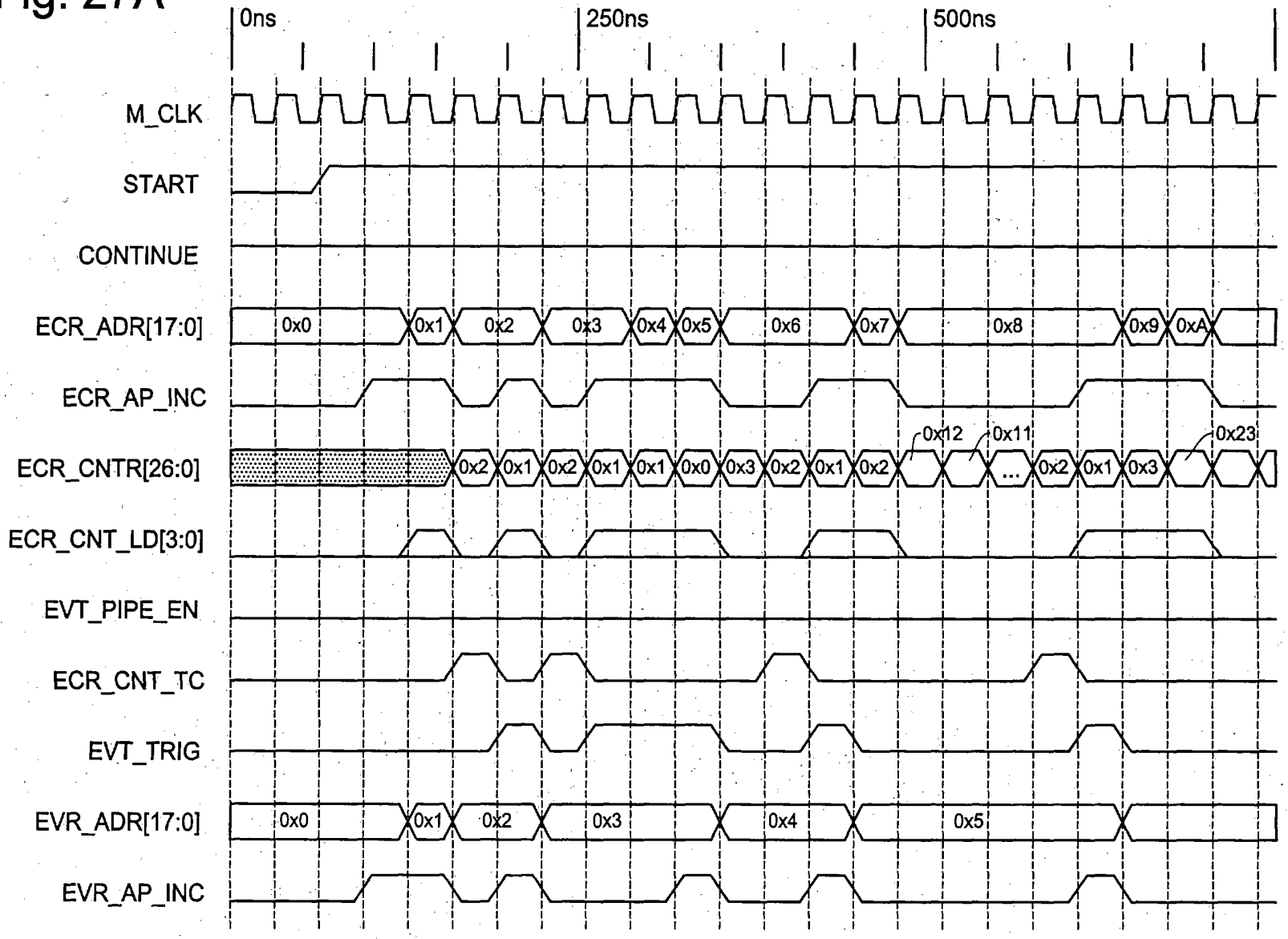

0ns
250ns
500ns
M_CLK
START
CONTINUE
ECR_ADR[17:0]
0x0
0x1
0x2
0x3
0x4
0x5
0x6
0x7
0x8
0x9
0xA
ECR_AP_INC
ECR_CNTR[26:0]
0x12
0x11
0x23
0x2
0x1
0x2
0x1
0x1
0x0
0x3
0x2
0x1
0x2
...
0x2
0x1
0x3
ECR_CNT_LD[3:0]
EVT_PIPE_EN
ECR_CNT_TC
EVT_TRIG
EVR_ADR[17:0]
0x0
0x1
0x2
0x3
0x4
0x5
EVR_AP_INC

Fig. 27B

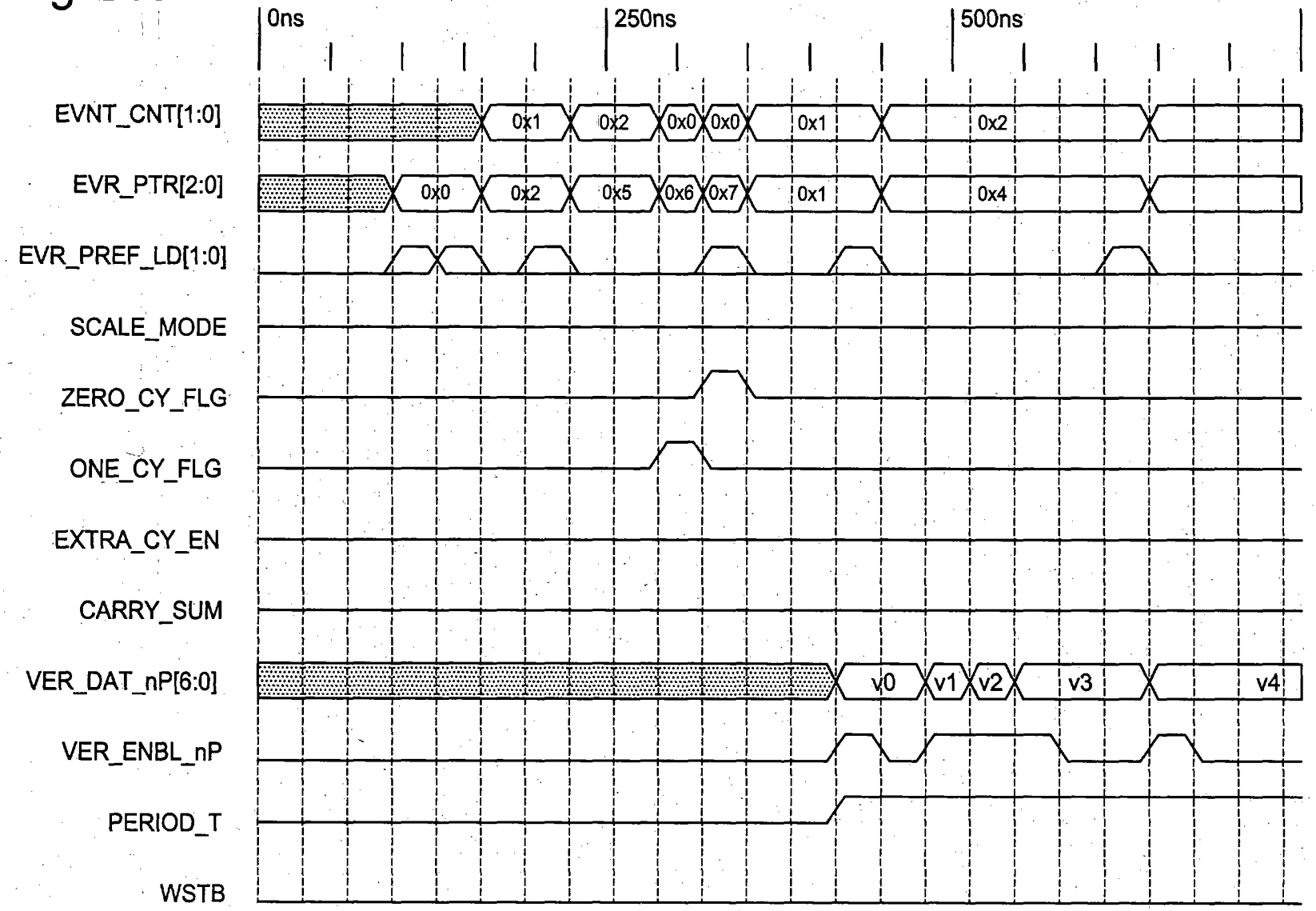

0ns
250ns
500ns
EVNT_CNT[1:0]
0x1
0x2
0x0
0x0
0x1
0x2
EVR_PTR[2:0]
0x0
0x2
0x5
0x6
0x7
0x1
0x4
EVR_PREF_LD[1:0]
SCALE_MODE
ZERO_CY_FLG
ONE_CY_FLG
EXTRA_CY_EN
CARRY_SUM
VER_DAT_nP[6:0]
v0
v1
v2
v3
v4
VER_ENBL_nP
PERIOD_T
WSTB

Fig. 28A

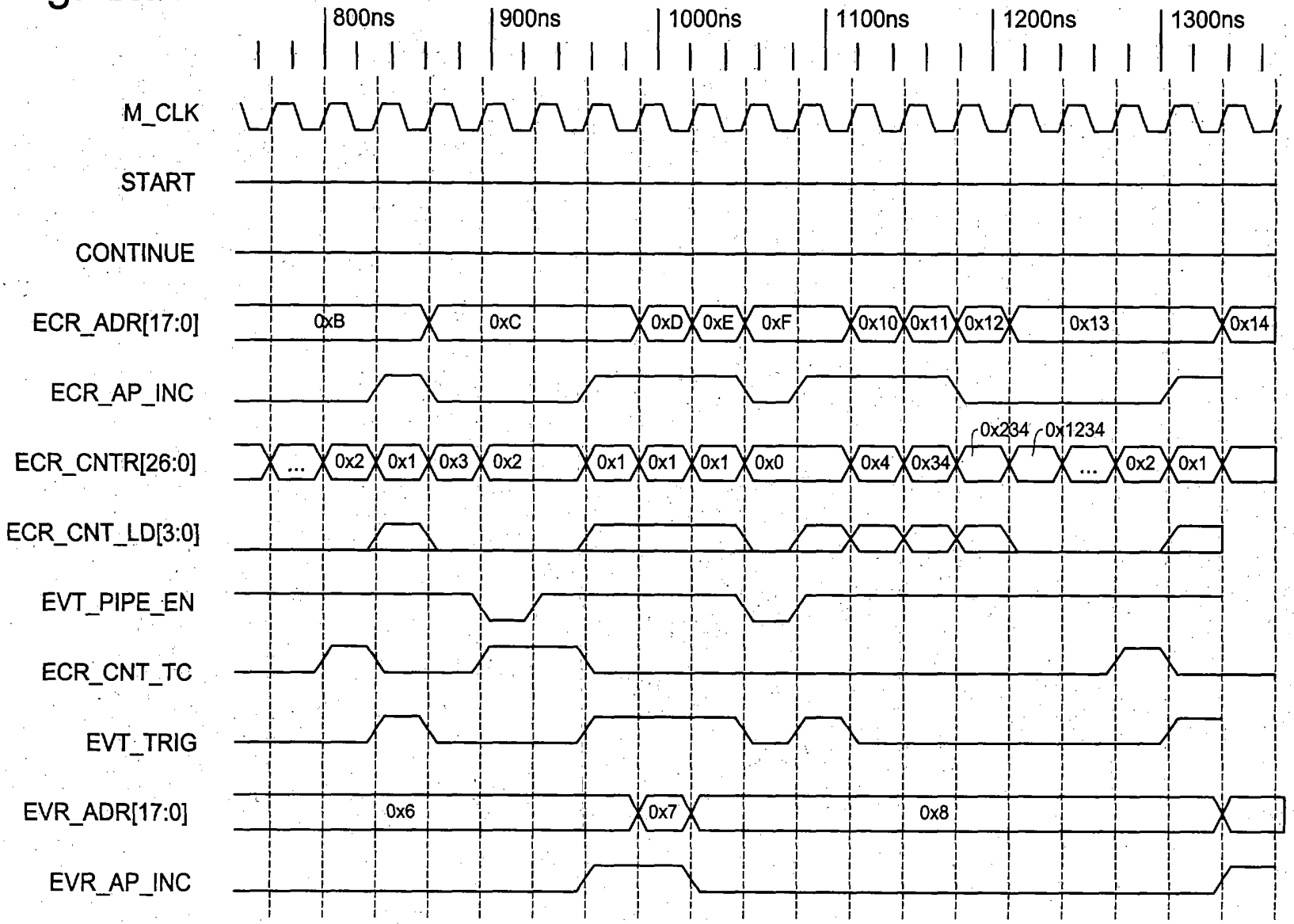

800ns
900ns
1000ns
1100ns
1200ns
1300ns
M_CLK
START
CONTINUE
ECR_ADR[17:0]
0xB
0xC
0xD
0xE
0xF
0x10
0x11
0x12
0x13
0x14
ECR_AP_INC
ECR_CNTR[26:0]
...
0x2
0x1
0x3
0x2
0x1
0x1
0x1
0x0
0x4
0x34
0x234
0x1234
...
0x2
0x1
ECR_CNT_LD[3:0]
EVT_PIPE_EN
ECR_CNT_TC
EVT_TRIG
EVR_ADR[17:0]
0x6
0x7
0x8
EVR_AP_INC

Fig. 28B

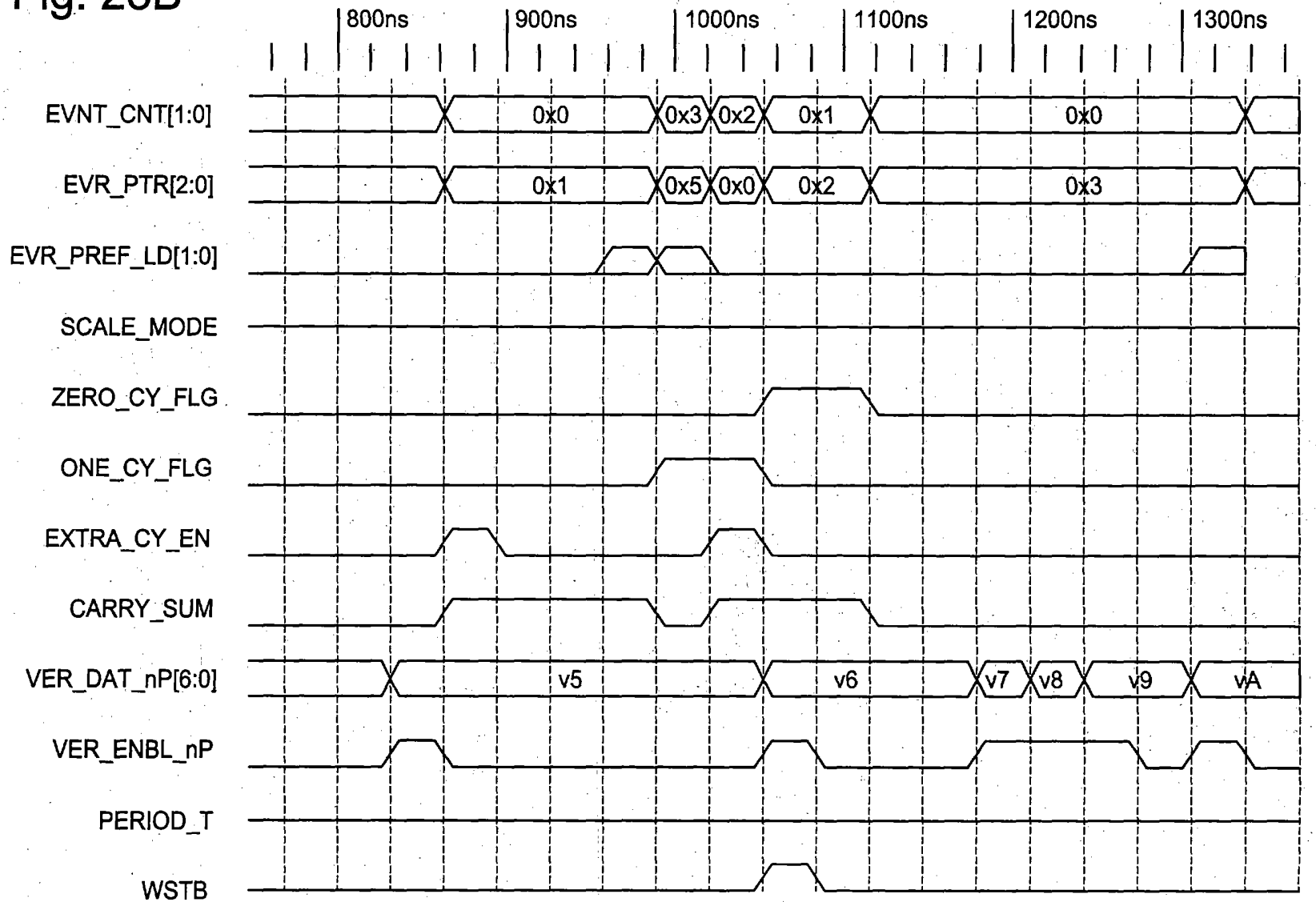

800ns
900ns
1000ns
1100ns
1200ns
1300ns
EVNT_CNT[1:0]
0x0
0x3
0x2
0x1
0x0
EVR_PTR[2:0]
0x1
0x5
0x0
0x2
0x3
EVR_PREF_LD[1:0]
SCALE_MODE
ZERO_CY_FLG
ONE_CY_FLG
EXTRA_CY_EN
CARRY_SUM
VER_DAT_nP[6:0]
v5
v6
v7
v8
v9
vA
VER_ENBL_nP
PERIOD_T
WSTB

Fig. 29A

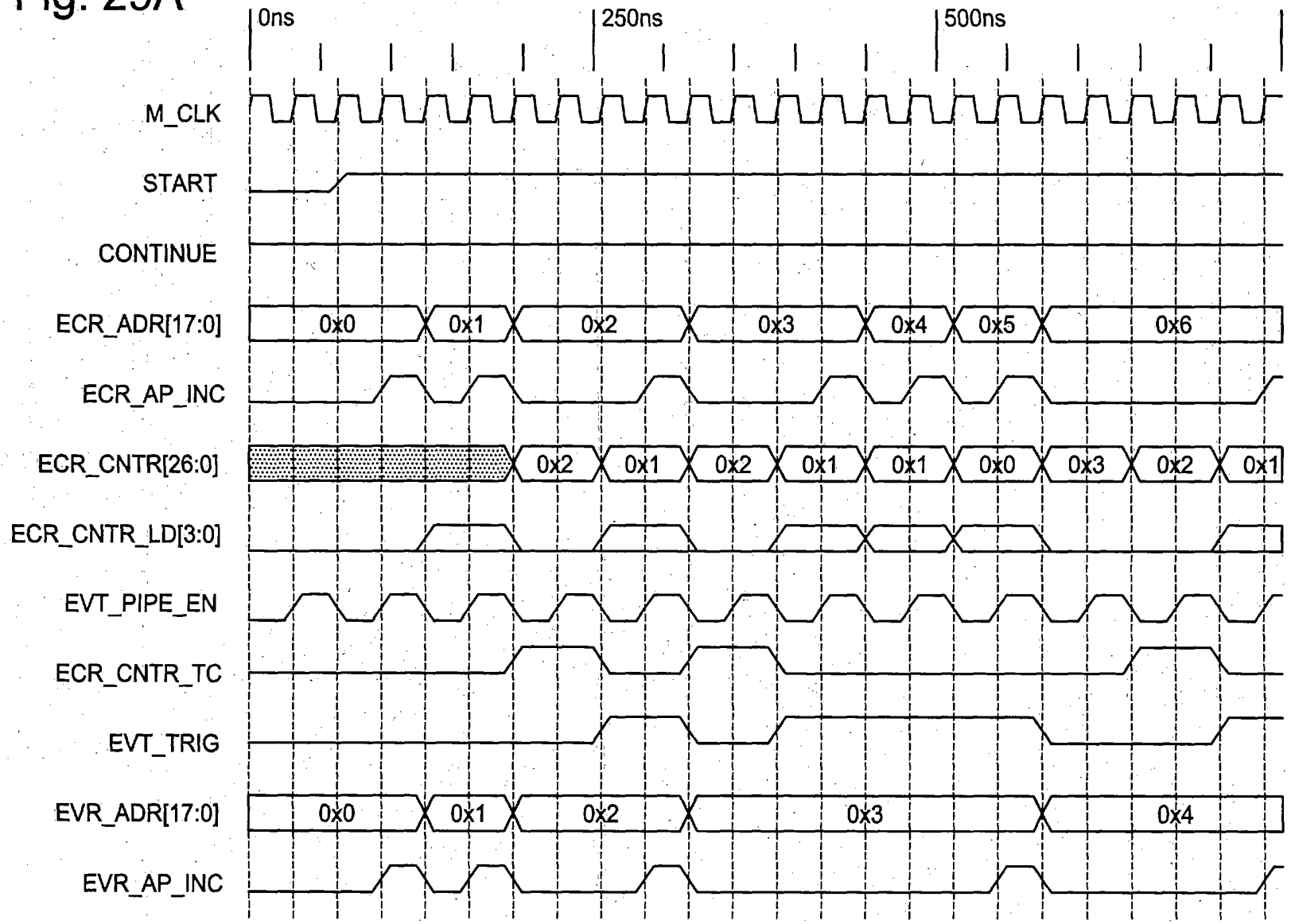

0ns
250ns
500ns
M_CLK
START
CONTINUE
ECR_ADR[17:0]
0x0
0x1
0x2
0x3
0x4
0x5
0x6
ECR_AP_INC
ECR_CNTR[26:0]
0x2
0x1
0x2
0x1
0x1
0x0
0x3
0x2
0x1
ECR_CNTR_LD[3:0]
EVT_PIPE_EN
ECR_CNTR_TC
EVT_TRIG
EVR_ADR[17:0]
0x0
0x1
0x2
0x3
0x4
EVR_AP_INC

Fig. 29B

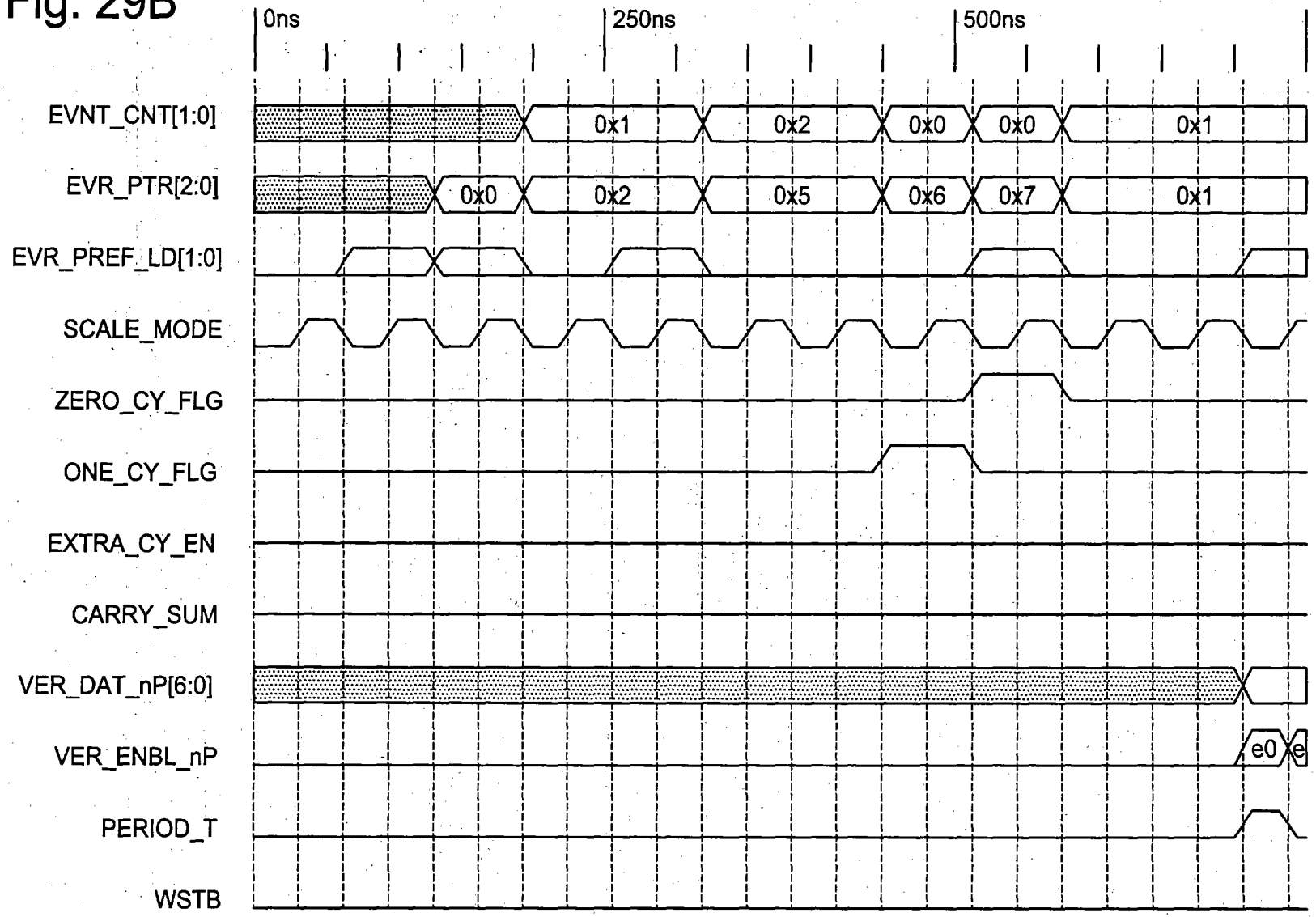

0ns
250ns
500ns
EVNT_CNT[1:0]
0x1
0x2
0x0
0x0
0x1
EVR_PTR[2:0]
0x0
0x2
0x5
0x6
0x7
0x1
EVR_PREF_LD[1:0]
SCALE_MODE
ZERO_CY_FLG
ONE_CY_FLG
EXTRA_CY_EN
CARRY_SUM
VER_DAT_nP[6:0]
VER_ENBL_nP
e0
e
PERIOD_T
WSTB

Fig. 30A

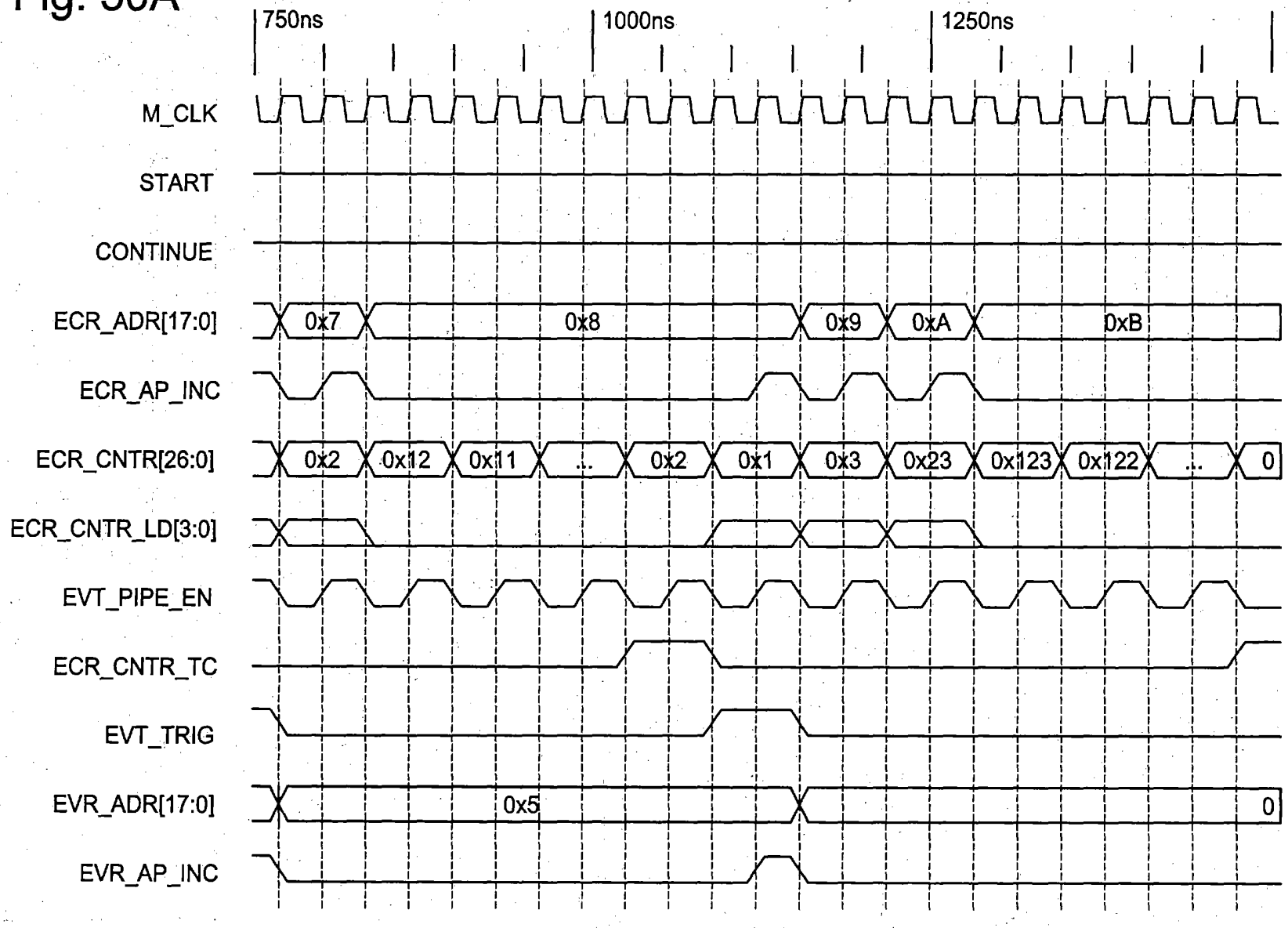

750ns
1000ns
1250ns
M_CLK
START
CONTINUE
ECR_ADR[17:0]
0x7
0x8
0x9
0xA
0xB
ECR_AP_INC
ECR_CNTR[26:0]
0x2
0x12
0x11
...
0x2
0x1
0x3
0x23
0x123
0x122
...
0
ECR_CNTR_LD[3:0]
EVT_PIPE_EN
ECR_CNTR_TC
EVT_TRIG
EVR_ADR[17:0]
0x5
0
EVR_AP_INC

Fig. 30B

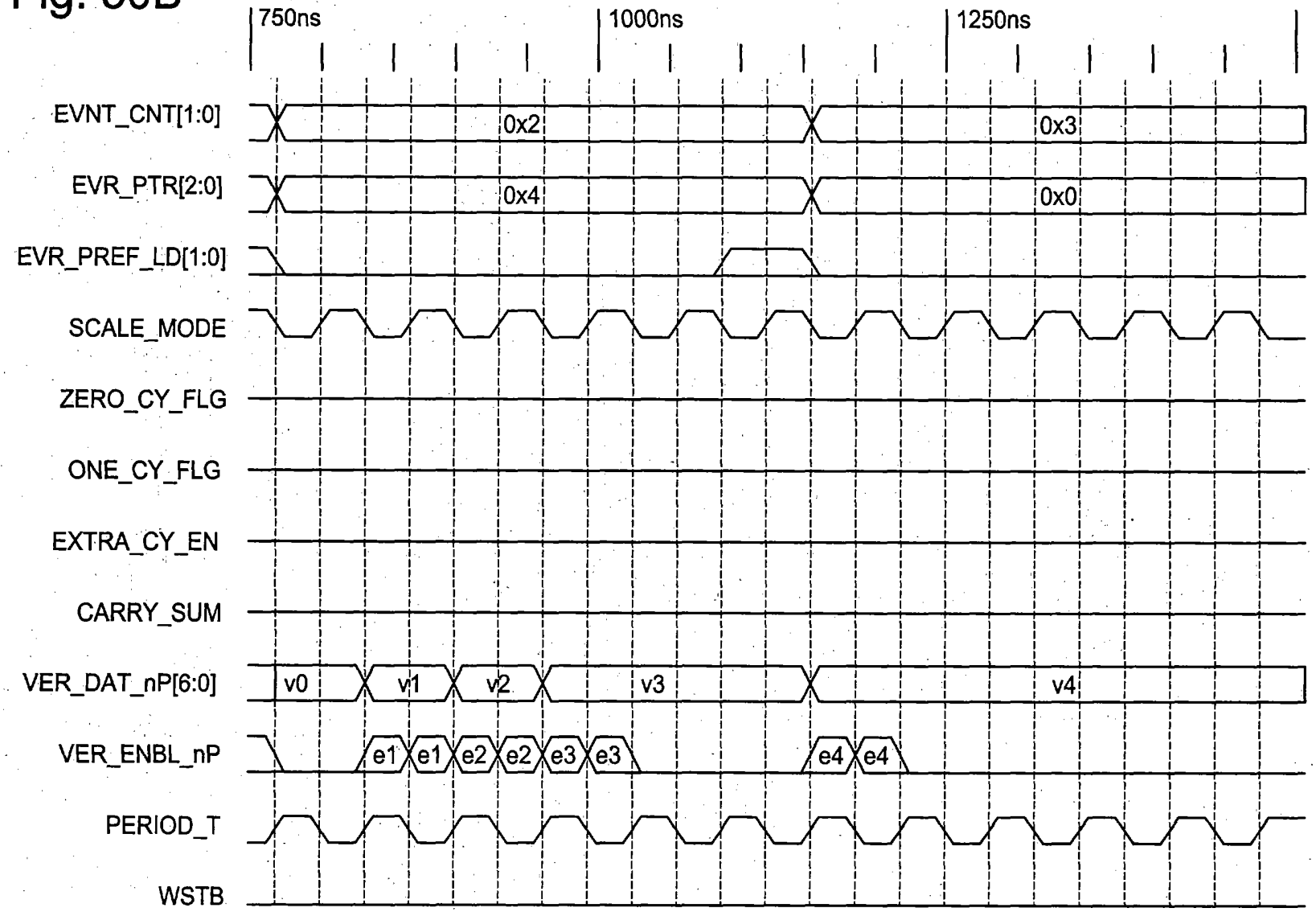

750ns
1000ns
1250ns
EVNT_CNT[1:0]
0x2
0x3
EVR_PTR[2:0]
0x4
0x0
EVR_PREF_LD[1:0]
SCALE_MODE
ZERO_CY_FLG
ONE_CY_FLG
EXTRA_CY_EN
CARRY_SUM
VER_DAT_nP[6:0]
v0
v1
v2
v3
v4
VER_ENBL_nP
e1
e1
e2
e2
e3
e3
e4
e4
PERIOD_T
WSTB

Fig. 31A

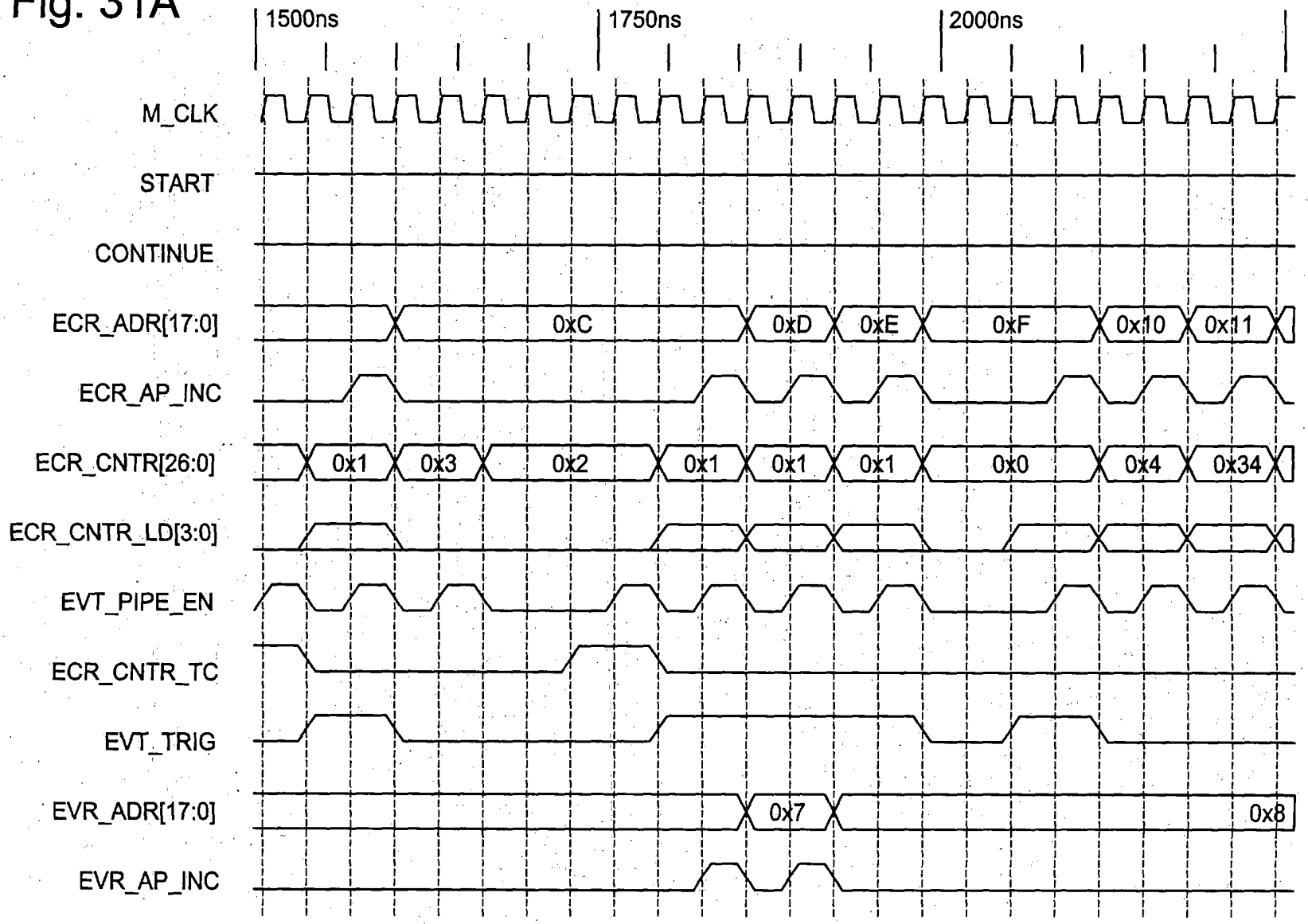
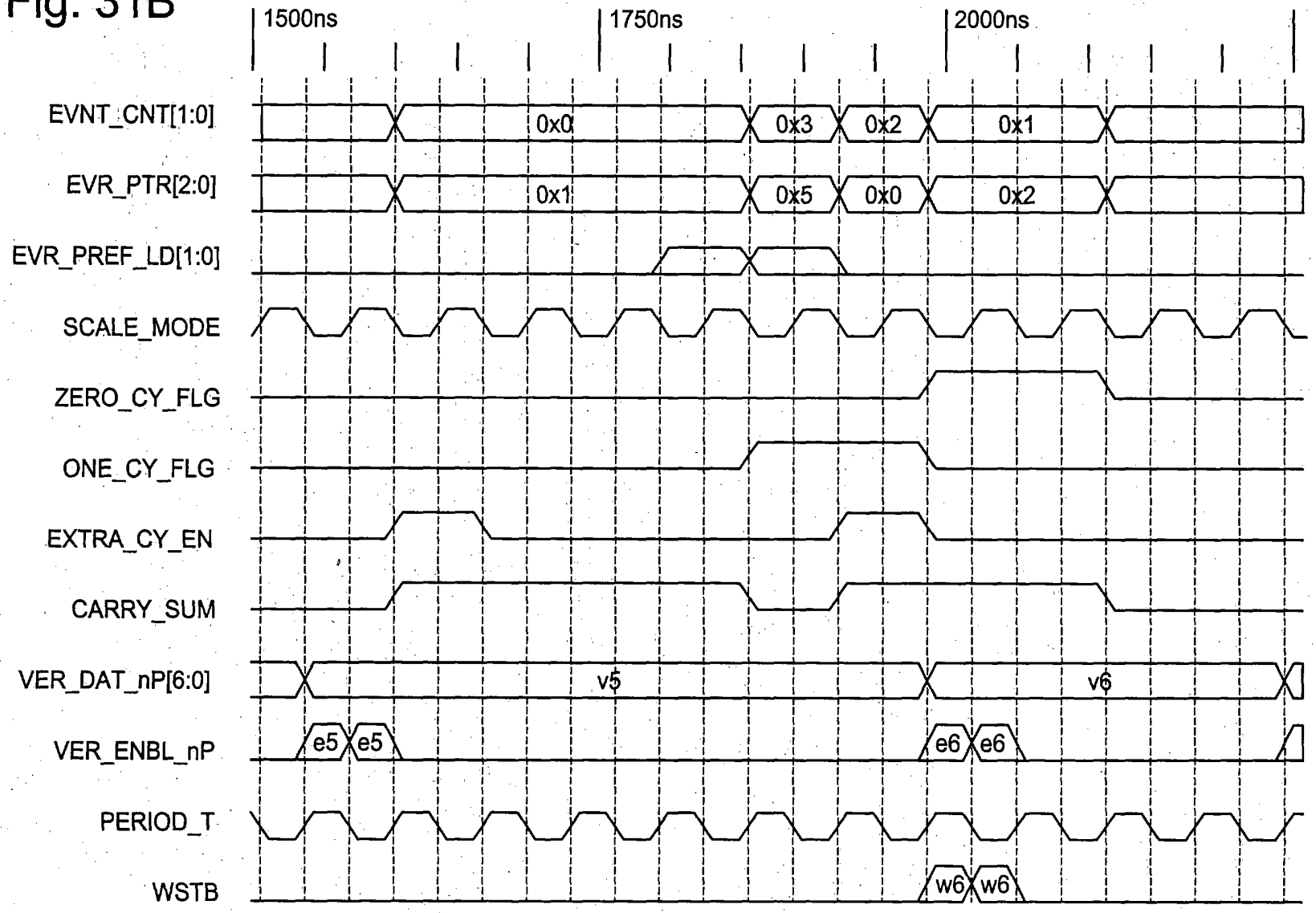

1500ns
1750ns
2000ns
M_CLK
START
CONTINUE
ECR_ADR[17:0]
0xC
0xD
0xE
0xF
0x10
0x11
ECR_AP_INC
ECR_CNTR[26:0]
0x1
0x3
0x2
0x1
0x1
0x1
0x0
0x4
0x34
ECR_CNTR_LD[3:0]
EVT_PIPE_EN
ECR_CNTR_TC
EVT_TRIG
EVR_ADR[17:0]
0x7
0x8
EVR_AP_INC

Fig. 31B


1500ns
1750ns
2000ns
EVNT_CNT[1:0]
0x0
0x3
0x2
0x1
EVR_PTR[2:0]
0x1
0x5
0x0
0x2
EVR_PREF_LD[1:0]
SCALE_MODE
ZERO_CY_FLG
ONE_CY_FLG
EXTRA_CY_EN
CARRY_SUM
VER_DAT_nP[6:0]
v5
v6
VER_ENBL_nP
e5
e5
e6
e6
PERIOD_T
WSTB
w6
w6